

PAGE	CONTENTS
1	COVER
2	BLOCK DIAGRAM
3	POWER DELIVERY
4	CLOCK DISTRIBUTION
5	REVISION HISTROY
6-10	AM3 CPU
11	CPU DECOUPLING
12	DDR3 DIMM A1/A2
13	DDR3 DIMM B1/B2
14	RS880 HT LINK
15	RS880 PCIE
16	RS880 SYSTEM
17	RS880 POWER&SBD_MEM
18	CLK GEN--RTM880N-793
19	SB850/810-PCIE/PCI/CPU/LPC
20	SB850/810-ACPI/GPIO/USB/AUD
21	SB850/810-SATA/IDE/HWM/SPI
22	SB850/810-POWER&DECOUPLING
23	SB850/810-STRAP
24	CRT & DVI & HDMI
25	PCI-E X16/X1 SLOT
26	PCI SLOT 1/2
27	IDE ATA 133
28	USB/1394 CONN
29	CODEC ALC888
30	AUDIO CONNECTOR
31	SUPER I/O IT8721
32	H/W MON / FAN CONTROL
33	PS2 CONN / MH
34	COMPORT/PRINTER HEADER
35	ATX PWR / FRONT PANEL / LED
36	OVER VOLTAGE/PSI LED
37	FRONT USB
38	PWRGD
39	VCC_CORE DC-DC CONVER
40	MEM POWER
41	NB/SB CORE POWER
42	REL8111DL/8102EL
43	BOM

**Model Name :** A89GA-M3T  
**Marketing name :** TA890GXE

**VER: 5.3**

**CPU :**

AM3, Including AthlonII / Phenom II/ Sempron

**System Chipset :**

AMD RS880D

AMD SB850

**On Board Chip :**

Clock Gen. -- RealTek RTM880N-793

Azalia Codec -- RealTek ALC892

GigaBit Lan -- RealTek RTL8111DL

PWM Controller -- CHL2399A

eSATA Controller -- PI3EQX4951B TQFN20

Super I/O -- IT8721FBX

SPI Flash 8Mb

**Main Memory :**

4 Channel DDR 3 \* 4 (Max 8GB)

**Expansion Slot :**

PCI Express x16 Slot \* 1

PCI Express x1 Slot \* 1

PCI Slot \* 2

**Heatsink :**

NB: NBHS-A89GA

SB: SB SMALL-AMD

MOS: MOSHS-A89GA


**I/O Pannel :**

47-RIOBRACKET-83

**PCB SIZE :**

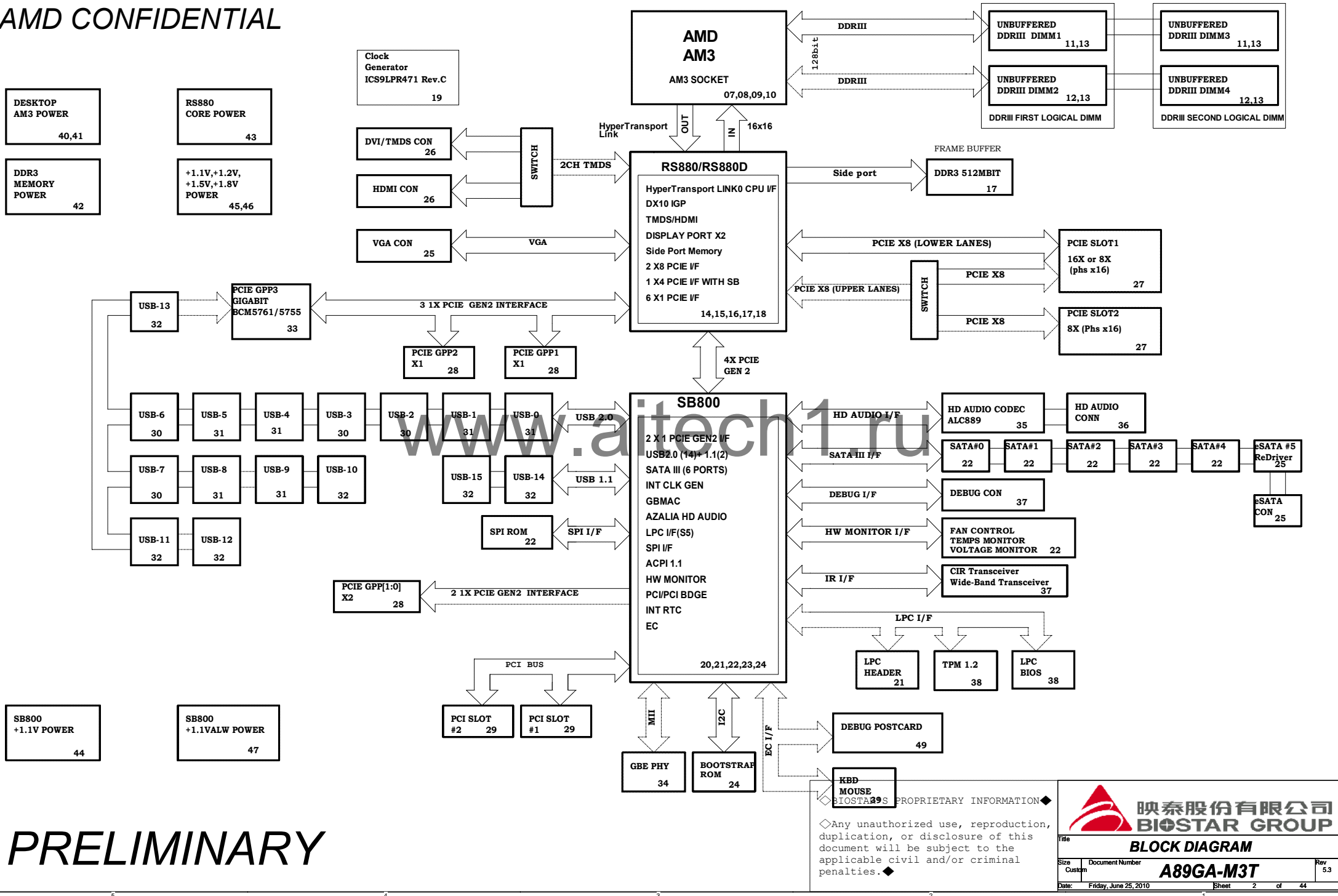
243.84 X 243.84mm

4-layers-1080

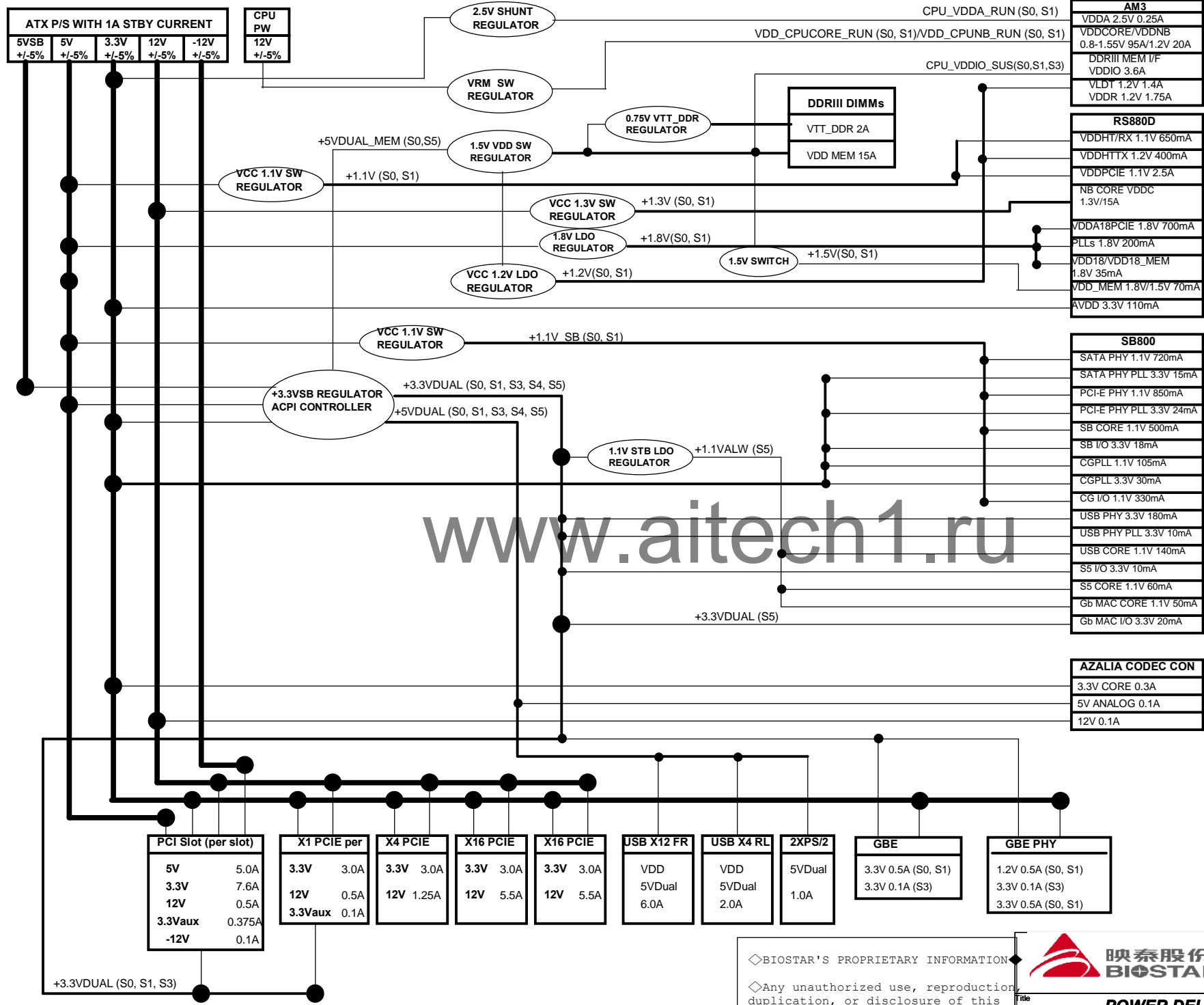
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<b>HW Leader:</b>		<b>Date:</b>	
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AMD CONFIDENTIAL

# TARPON (AM3+RS880D+SB800) CUSTOMER DESKTOP REFERENCE DESIGN



PRELIMINARY



AM3
VDDA 2.5V 0.25A
VDDCORE/VDDNB 0.8-1.55V 95A/1.2V 20A
DDRIII MEM I/F VDDIO 3.6A
VLDI 1.2V 1.4A
VDDR 1.2V 1.75A

RS880D
VDDHT/RX 1.1V 650mA
VDDHTTX 1.2V 400mA
VDDPCIE 1.1V 2.5A
NB CORE VDDC 1.3V/15A
VDDA18PCIE 1.8V 700mA
PLLs 1.8V 200mA
VDD18/VDD18_MEM 1.8V 35mA
VDD_MEM 1.8V/1.5V 70mA
AVDD 3.3V 110mA

SB800
SATA PHY 1.1V 720mA
SATA PHY PLL 3.3V 15mA
PCI-E PHY 1.1V 850mA
PCI-E PHY PLL 3.3V 24mA
SB CORE 1.1V 500mA
SB I/O 3.3V 18mA
CGPLL 1.1V 105mA
CGPLL 3.3V 30mA
CG I/O 1.1V 330mA
USB PHY 3.3V 180mA
USB PHY PLL 3.3V 10mA
USB CORE 1.1V 140mA
S5 I/O 3.3V 10mA
S5 CORE 1.1V 60mA
Gb MAC CORE 1.1V 50mA
Gb MAC I/O 3.3V 20mA

AZALIA CODEC CON
3.3V CORE 0.3A
5V ANALOG 0.1A
12V 0.1A

PCI Slot (per slot)
5V 5.0A
3.3V 7.6A
12V 0.5A
3.3Vaux 0.375A
-12V 0.1A

X1 PCIE per
3.3V 3.0A
12V 0.5A
3.3Vaux 0.1A

X4 PCIE
3.3V 3.0A
12V 1.25A

X16 PCIE
3.3V 3.0A
12V 5.5A

X16 PCIE
3.3V 3.0A
12V 5.5A

USB X12 FR
VDD 5VDual 6.0A


USB X4 RL
VDD 5VDual 2.0A

2XPS/2
5VDual 1.0A

GBE
3.3V 0.5A (S0, S1)
3.3V 0.1A (S3)

GBE PHY
1.2V 0.5A (S0, S1)
3.3V 0.1A (S3)
3.3V 0.5A (S0, S1)

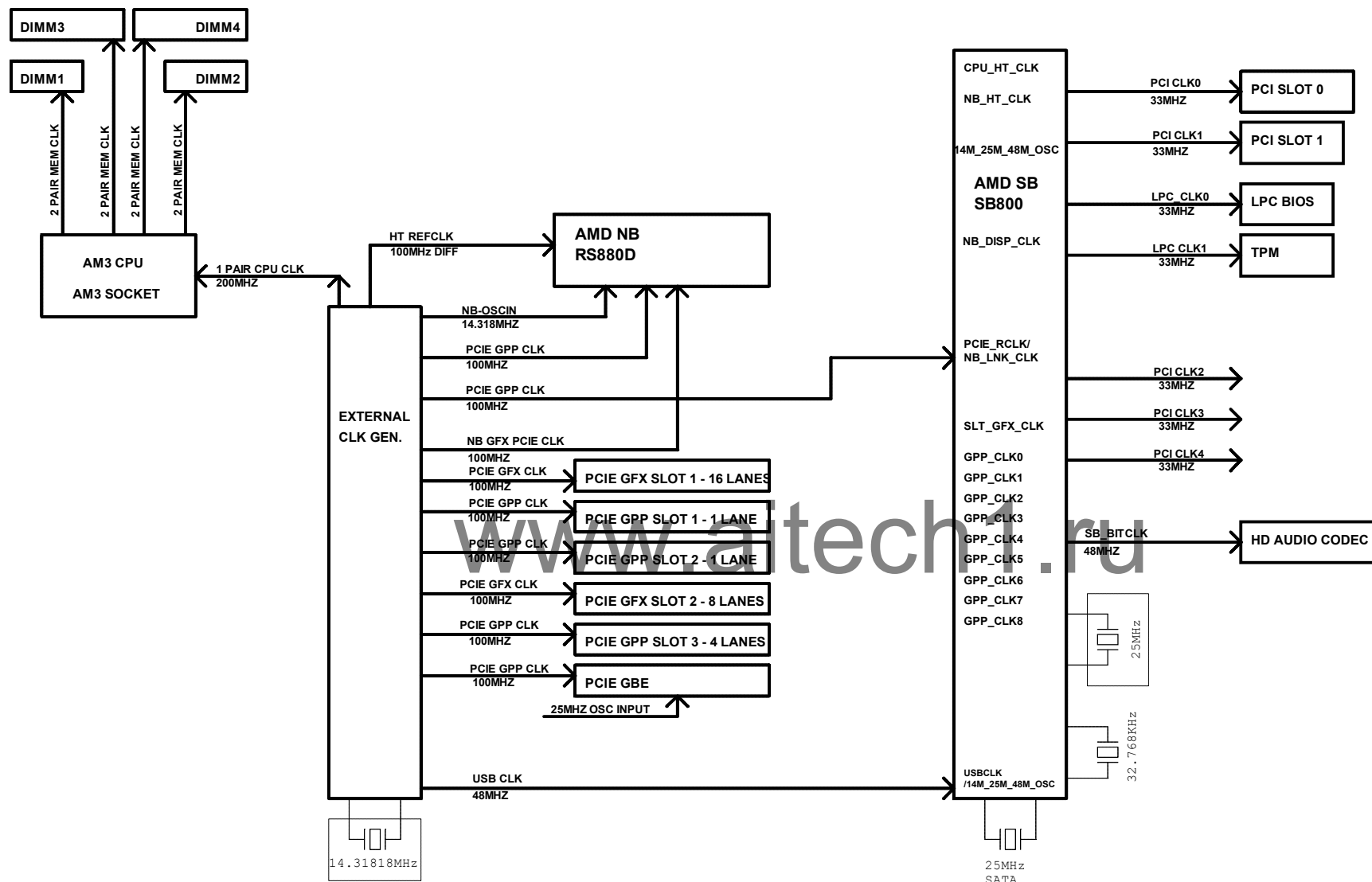
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External clock mode

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Date: Friday, June 25, 2010 Sheet 4 of 44



Date	Rev	Description
20010-03-25	5.2	1. PR(43 ,54 ,64 ,52 ,124) 2.7 Ohm 0805 -----> 0 Ohm 0805 "UGATE resister change" 2. PR(96 ,97 ,98 ,99 ,108) 1 Ohm 0805 -----> 0 Ohm 0805 "PHASE resister change" 3. R190 30K Ohm 0402 -----> 10K Ohm 0402 "CPUNB HW monitor resister change" 4. Board ID 党蚬蚬 ,001 5. BIOS ?党蚬蚬Chil PWM code
20010-04-15	5.2	CHANGE ALC892R TO ALC892,DeleteAR72,Add AR16,
20010-04-19	5.2	change MOSFET from ON to NIKO
20010-04-21	5.2	change NB HEATSINK
20010-05-28	0.53	PCIE 1X,16X signals ref GND蚬蚬decrease 1X signal length change eSATA Re-driver IC
20010-05-28	5.3	1.change GPP_CLK to CLK GEN 12,13PIN, change LAN GBE_CLK to CLK GEN 14,15PIN 2.change BOARD ID to 0 0 1

www.aitech1.ru

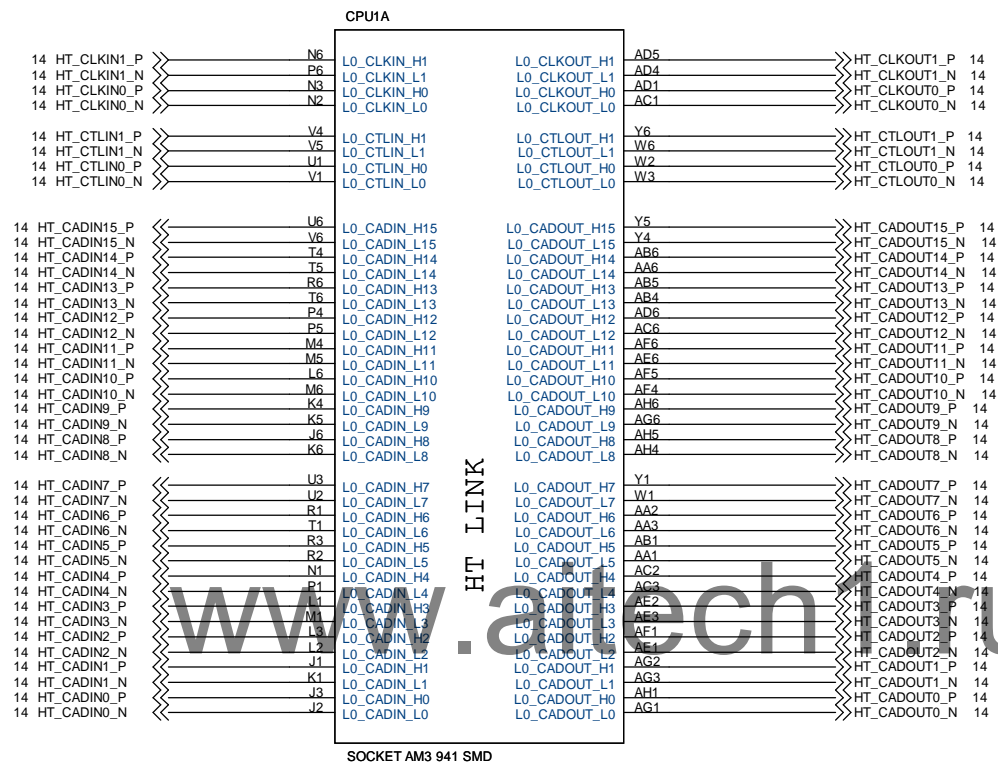
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Date: Friday, June 25, 2010		
Sheet 5 of 44		

# HyperTransport



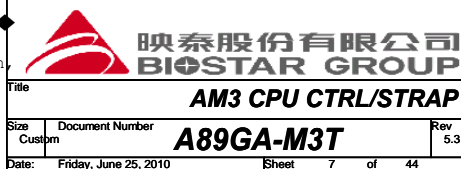
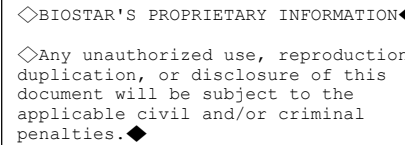
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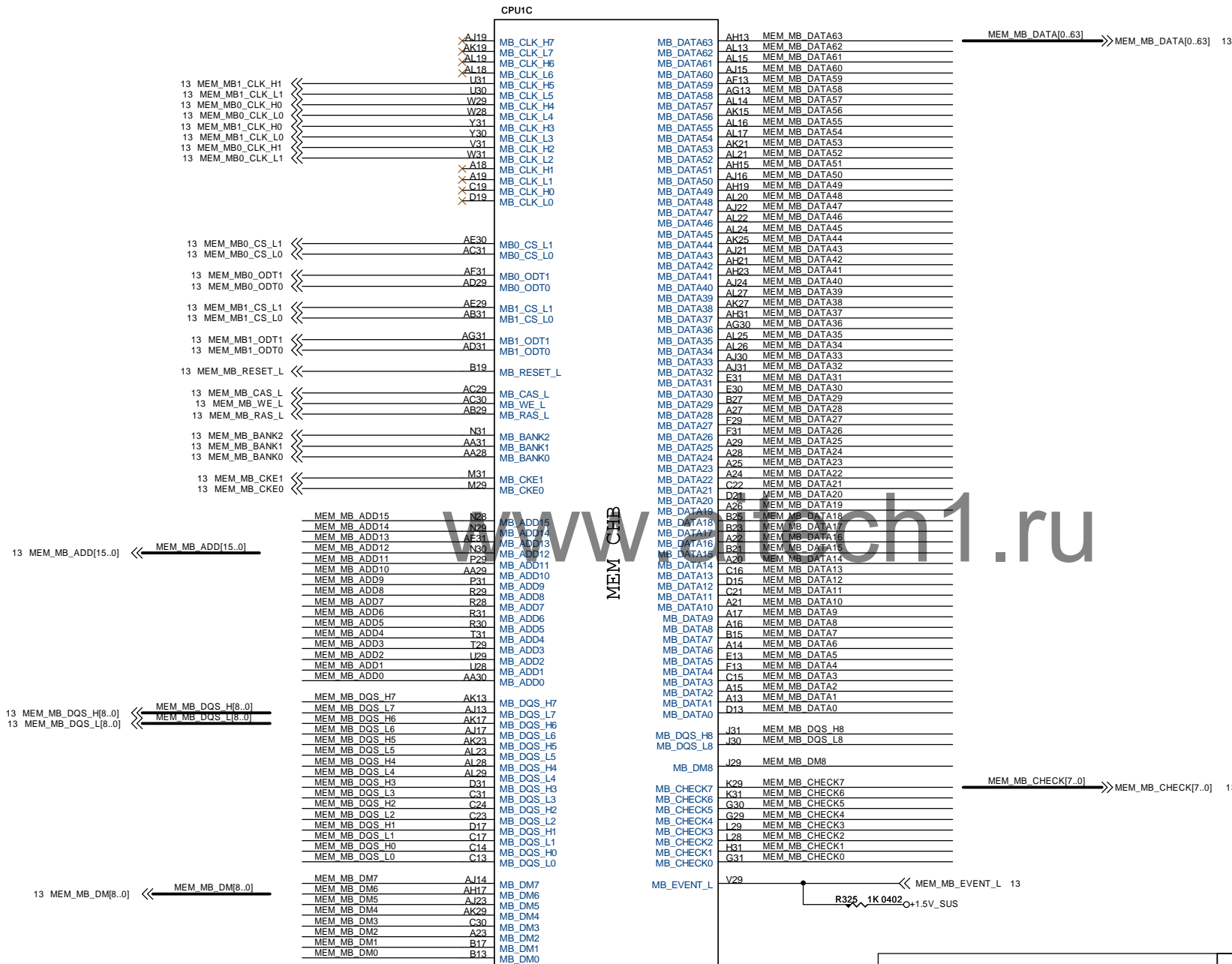


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			Rev 5.3




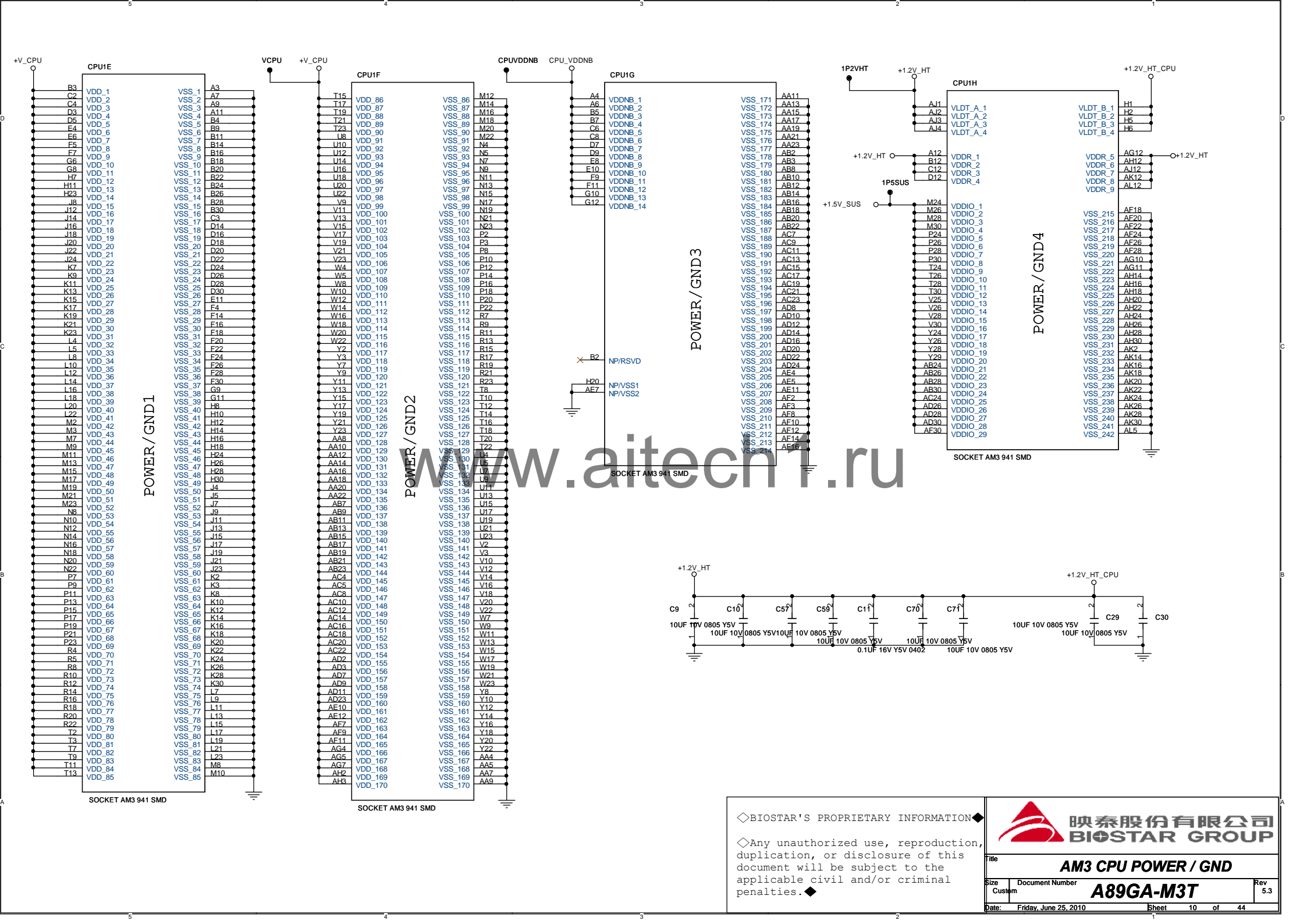




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Date:	Friday, June 25, 2010	Sheet	9 of 44



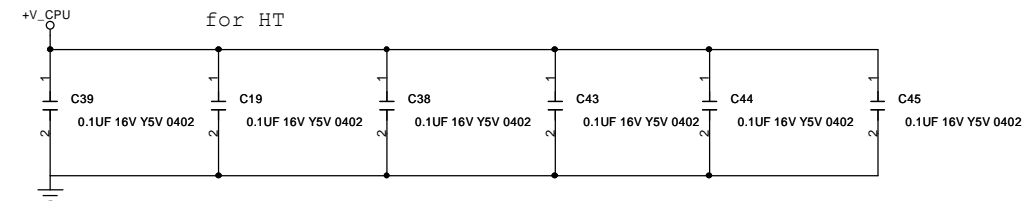
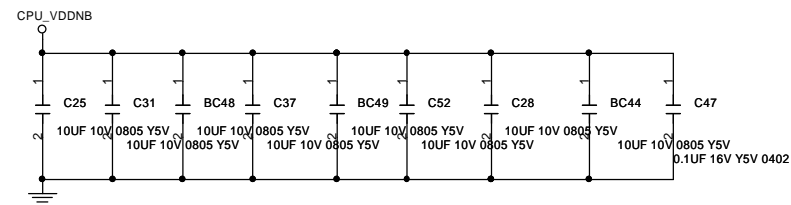
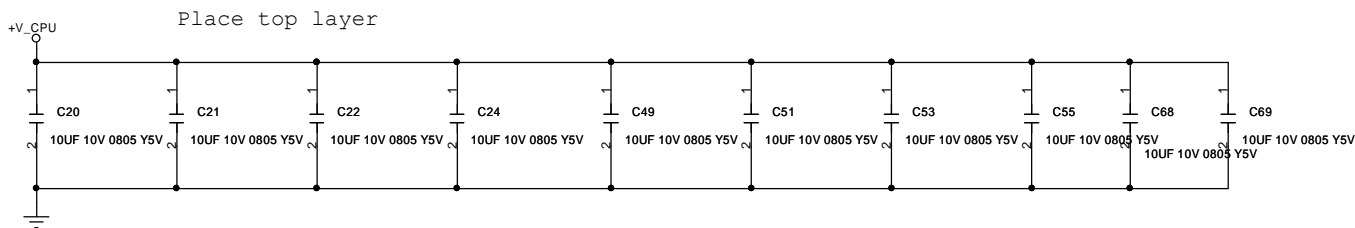
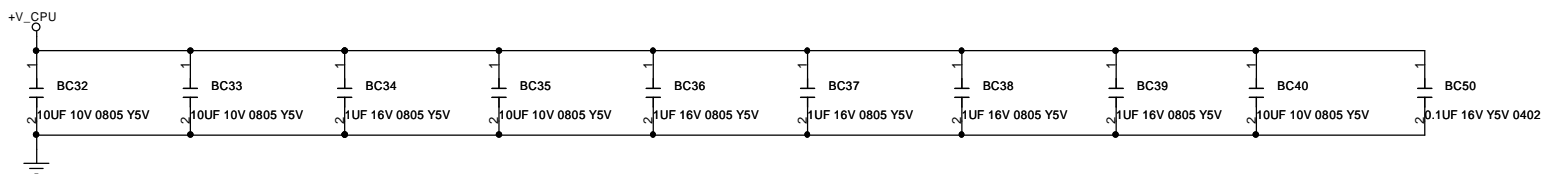
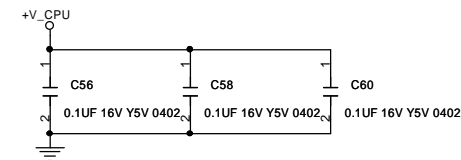
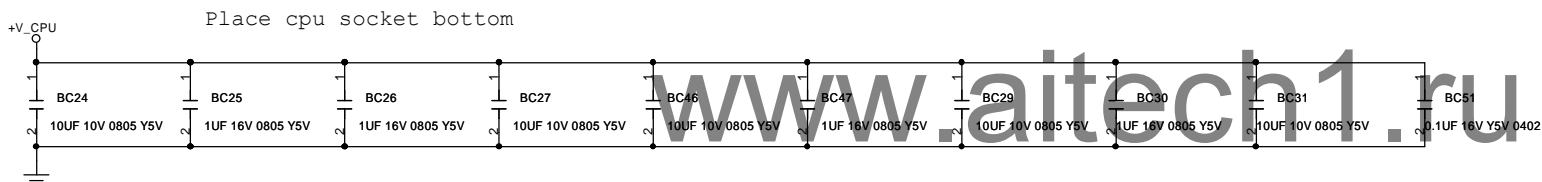
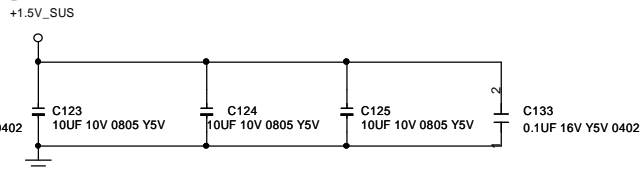
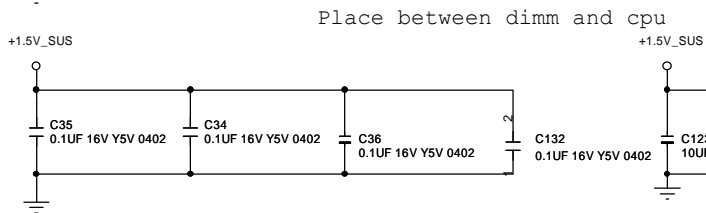
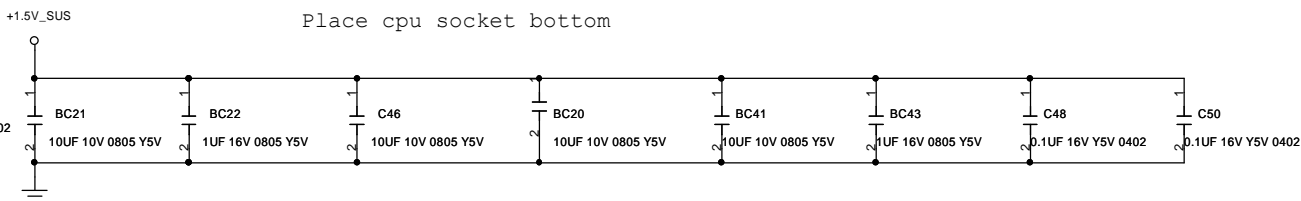
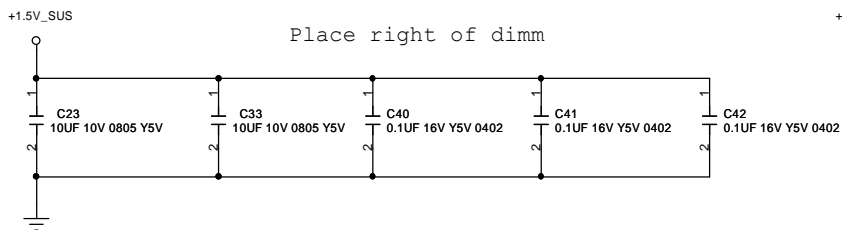
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Custom				
Date:	Friday, June 25, 2010	Sheet	10	of 44



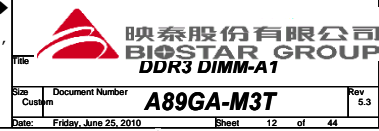
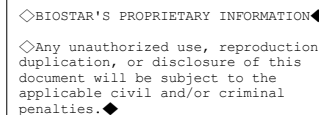
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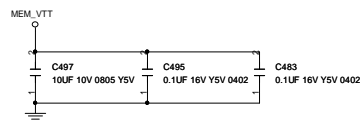
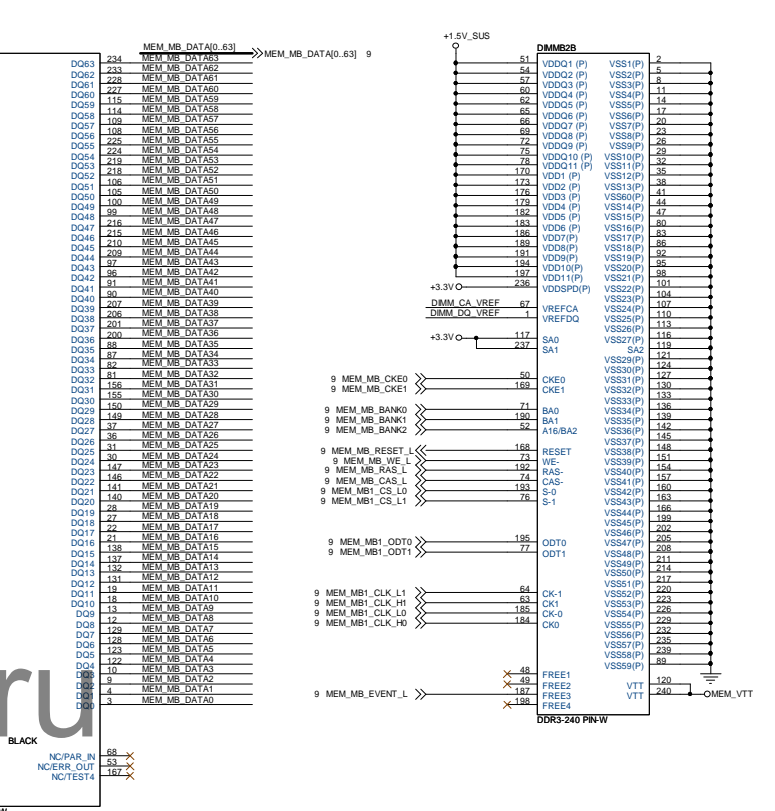
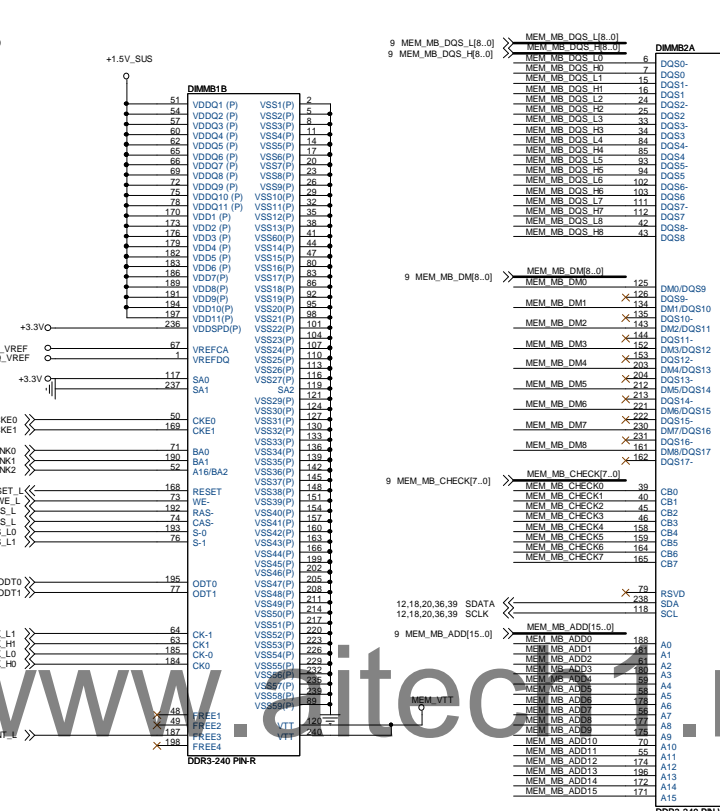


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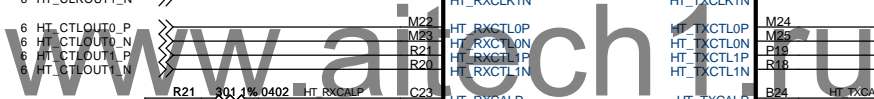


## DIMMB2



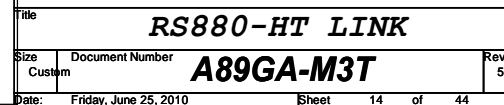
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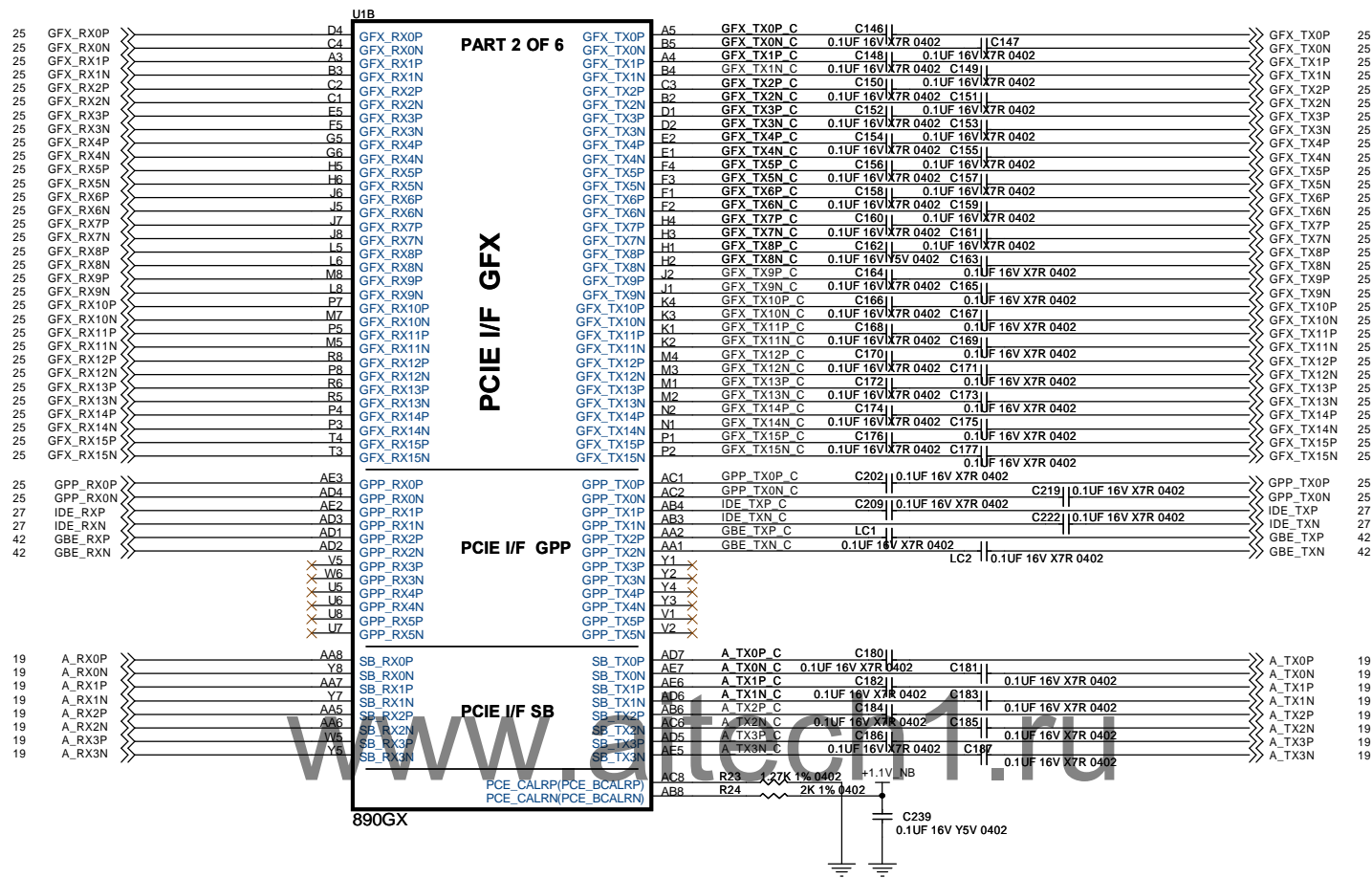




SIGNALS	RX740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP HT_TXCALN	100R	1.21K	301R

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# RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

	RS740	RX780/RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

	RS740	RX780/RS780
GPP X4 CONNECTOR	GPP[2:0]	GPP[3:0]
GPP X1 CONNECTOR		GPP4
GIGABIT ETHERNET	GPP3	GPP5

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RS880 PCI-E

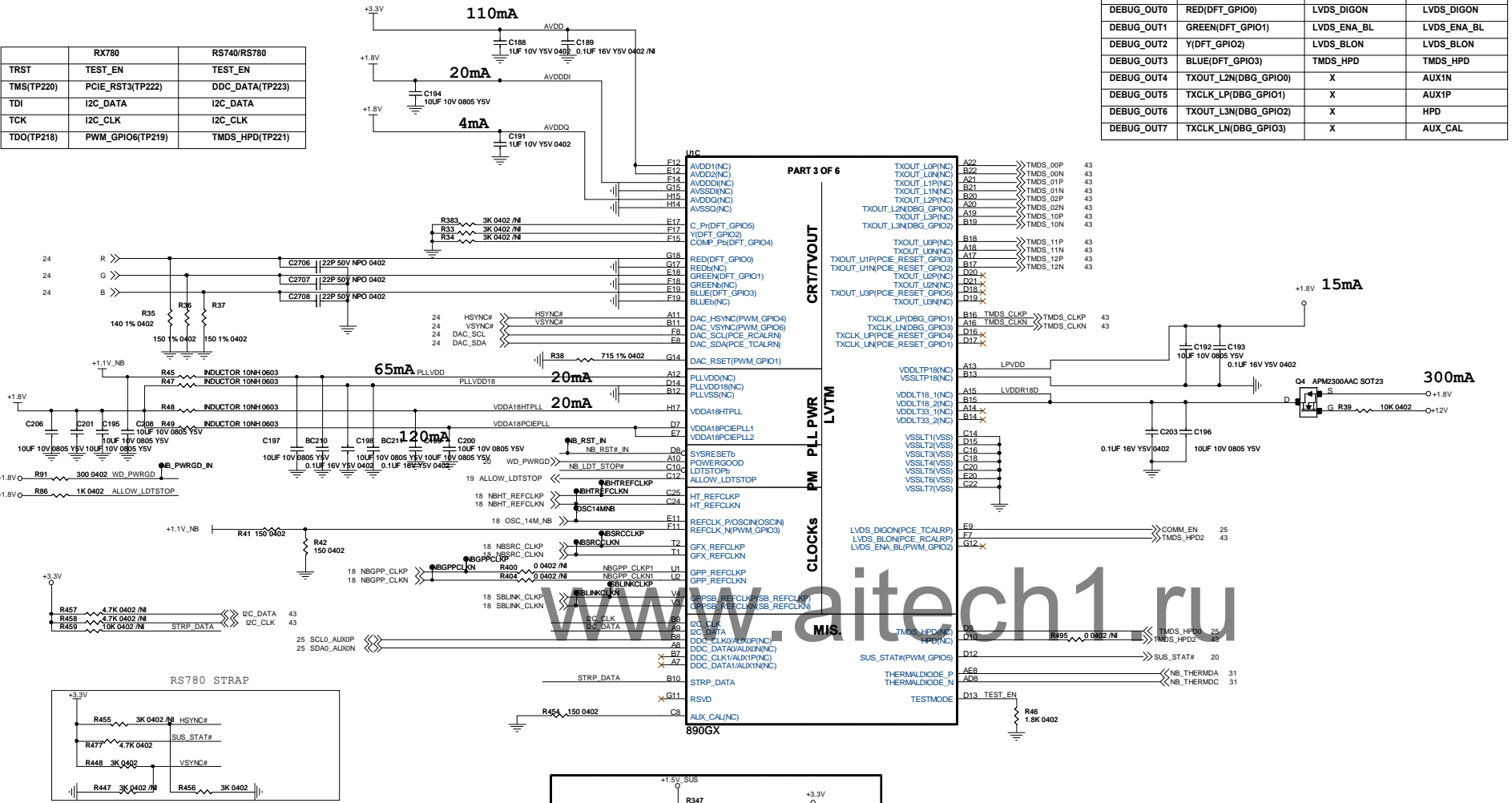
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Date: Friday, June 25, 2010 Sheet 15 of 44

# RX780/RS740/RS780 DEBUG PIN MAPPING

	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLOK	LVDS_BLOK
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMD5_HPD	TMD5_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

	RX780	RS740/RS780
TRST	TEST_EN	TEST_EN
TMS(TP220)	PCIE_RST3(TP222)	DDC_DATA(TP223)
TDI	I2C_DATA	I2C_DATA
TCK	I2C_CLK	I2C_CLK
TDO(TP218)	PWM_GPIO6(TP219)	TMD5_HPD(TP221)



**RS780D: STRAP\_DEBUG\_BUS\_GPIO\_ENABLE**

Enables the Test Debug Bus using GPIO and/or memory IO

1 : Disable

0 : Enable

RS780D: pin VSYNC

**RS780D: SIDE-PORT MEMORY ENABLE**

Enables Side port memory

1 : Disable

0 : Enable

RS780D: pin HSYNC

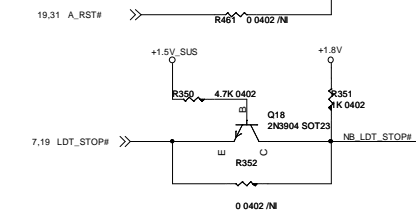
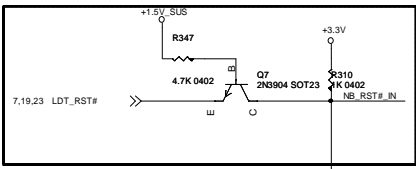
**RS780D: LOAD\_EEPROM\_STRAPS**

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EPROM straps and use Hardware Default Values

0 : I2C Master can load strap values from EPROM if connected, or use default values if not connected

RS780D: pin SUS\_STAT#



resolve ACC Function fail

RX740/RS740/RS780 difference table (Control signal)

	RS740	RX780	RS780
NB_PWRGD_IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDSTOP	OD	OD	OD/3.3V IN
OUT(default)/IN	3.3V IN	1.8V IN	3.3V IN/OD
SYSTEMRESETb	3.3V IN	1.8V IN	3.3V IN

VIH=1.4V

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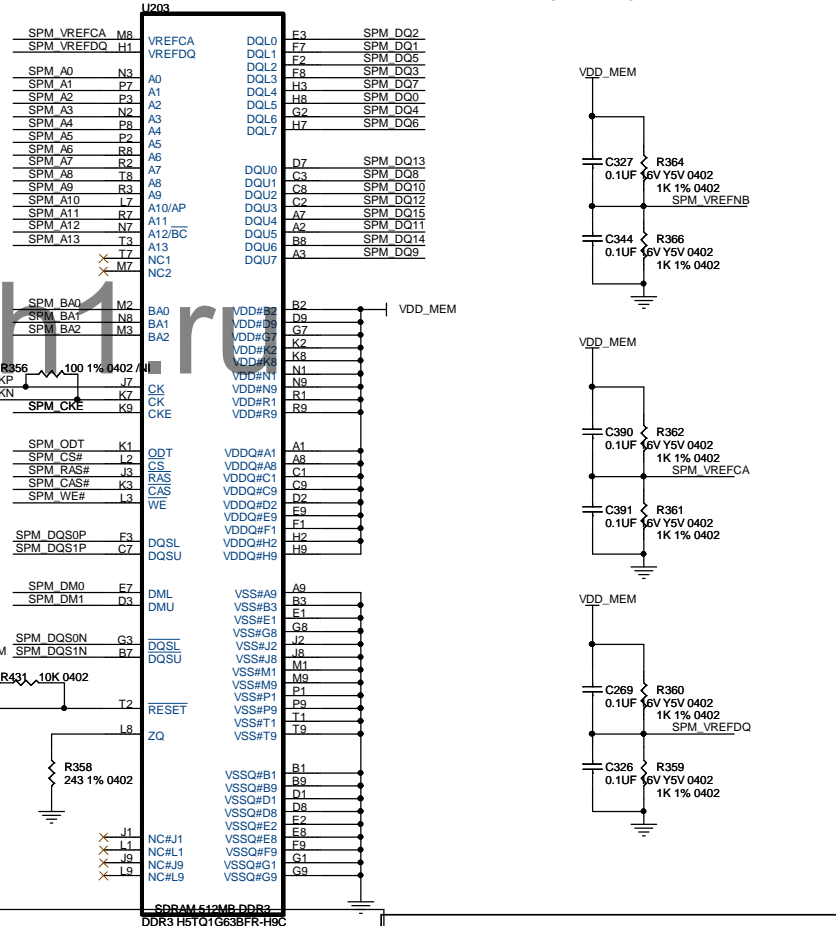
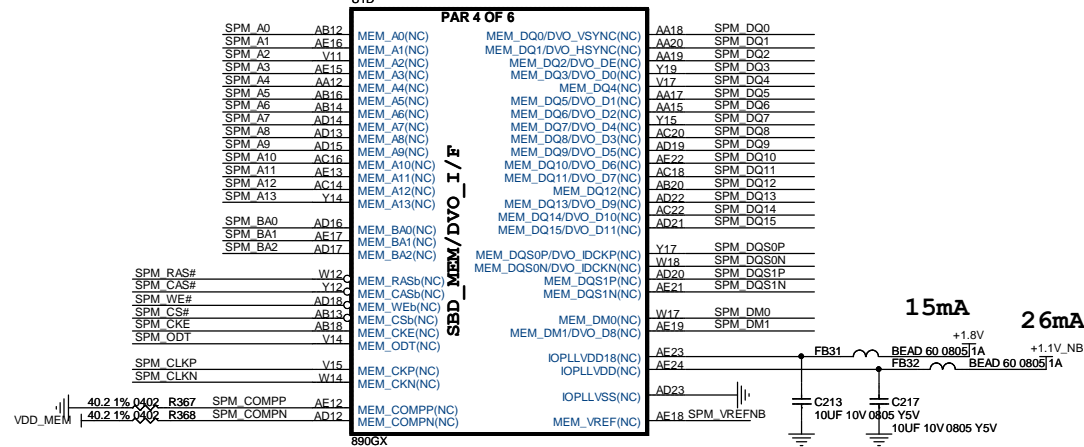
RS880 SYSTEM

A89GA-M3T

Rev 6.3

Date: Friday, June 25, 2010

Sheet 16 of 44

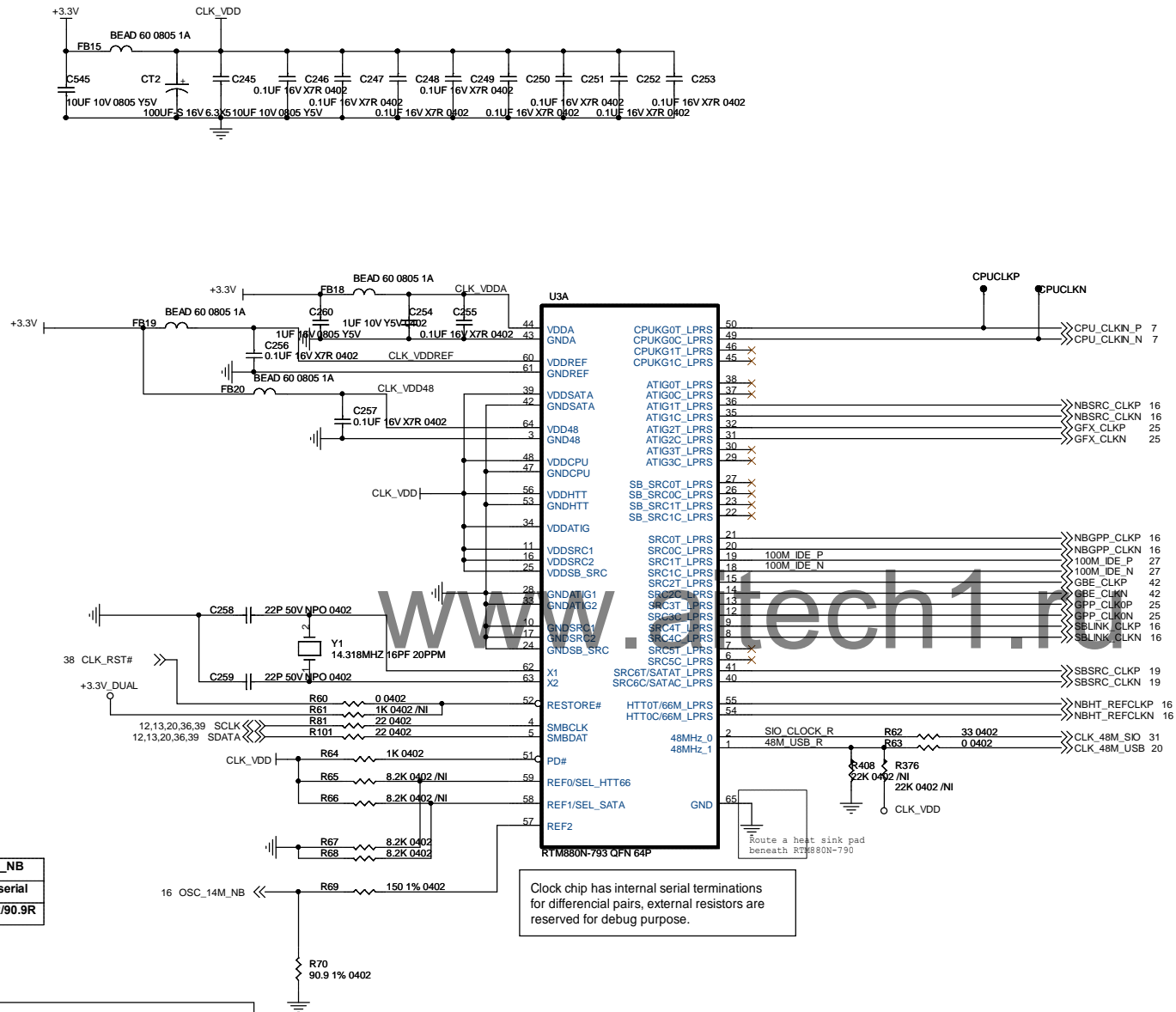


PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLT18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC

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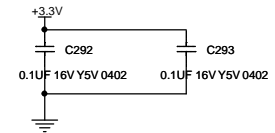
	OSC_14M_NB
RS740	3.3V 33R serial
RS780	1.1V 158R/90.9R

SEL_HTT66	1	66MHz 3.3V single ended HTT clock
	0*	100MHz differential HTT clock
SEL_SATA	1	100MHz non-spreading differential SATA clock
	0*	100MHz differential spreading SRC clock

\* default

NB CLOCK TABLE

NB CLOCKS	RS740	RS780
HT_REFCLKP	66MHz(Single End)	100MHz(Differential)
HT_REFCLKN	NC	
REFCLK_P	14MHz(Single End) 3.3V	14MHz(Single End) 3.3V
REFCLK_N	NC	
GFX_REFCLK	100MHz(Differential)	100MHz(Differential) IN/OUT
GPP_REFCLK	NC	NC or 100MHz(Diff) OUT
GPPSB_REFCLK	100MHz(Differential)	100MHz(Differential)



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**CLOCK RTM880N-793**

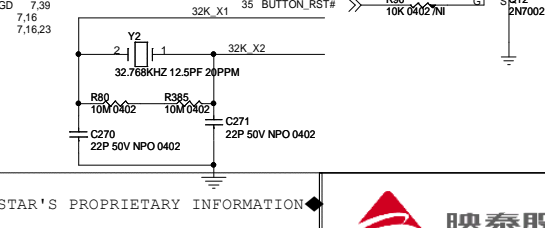
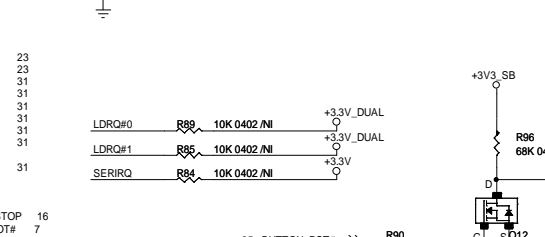
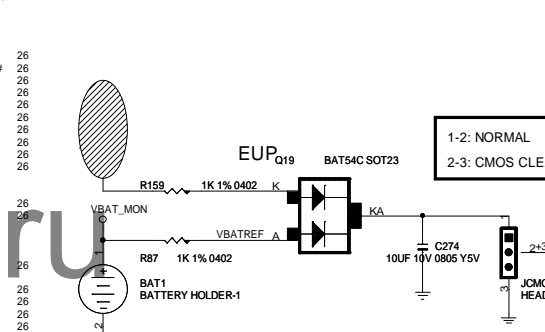
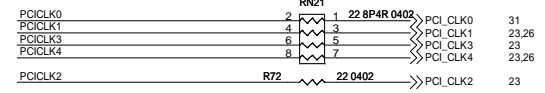
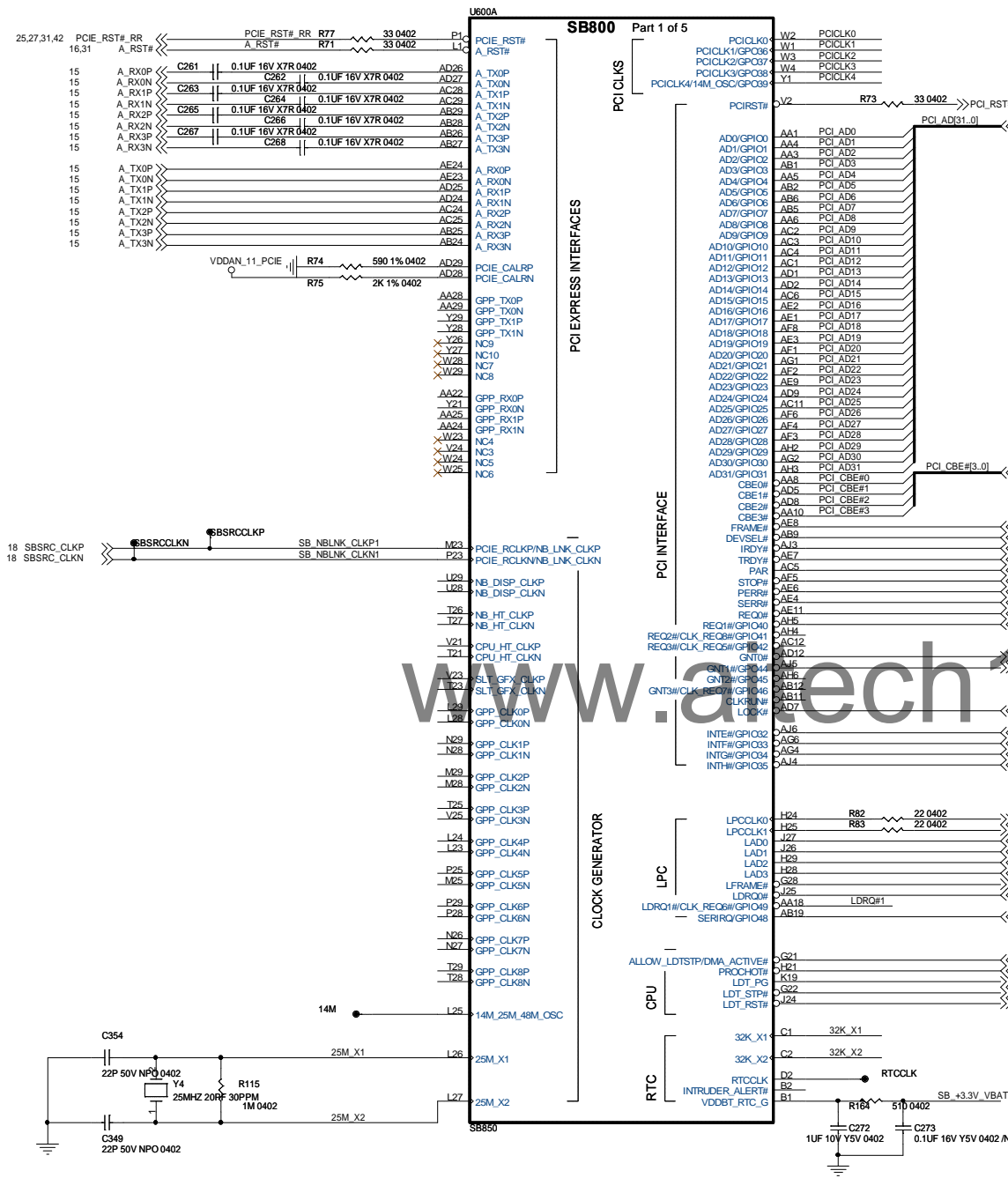
Size  
Custom

Date  
Friday, June 25, 2010

Document Number  
**A89GA-M3T**

Rev  
5.3

Sheet  
18 of 44



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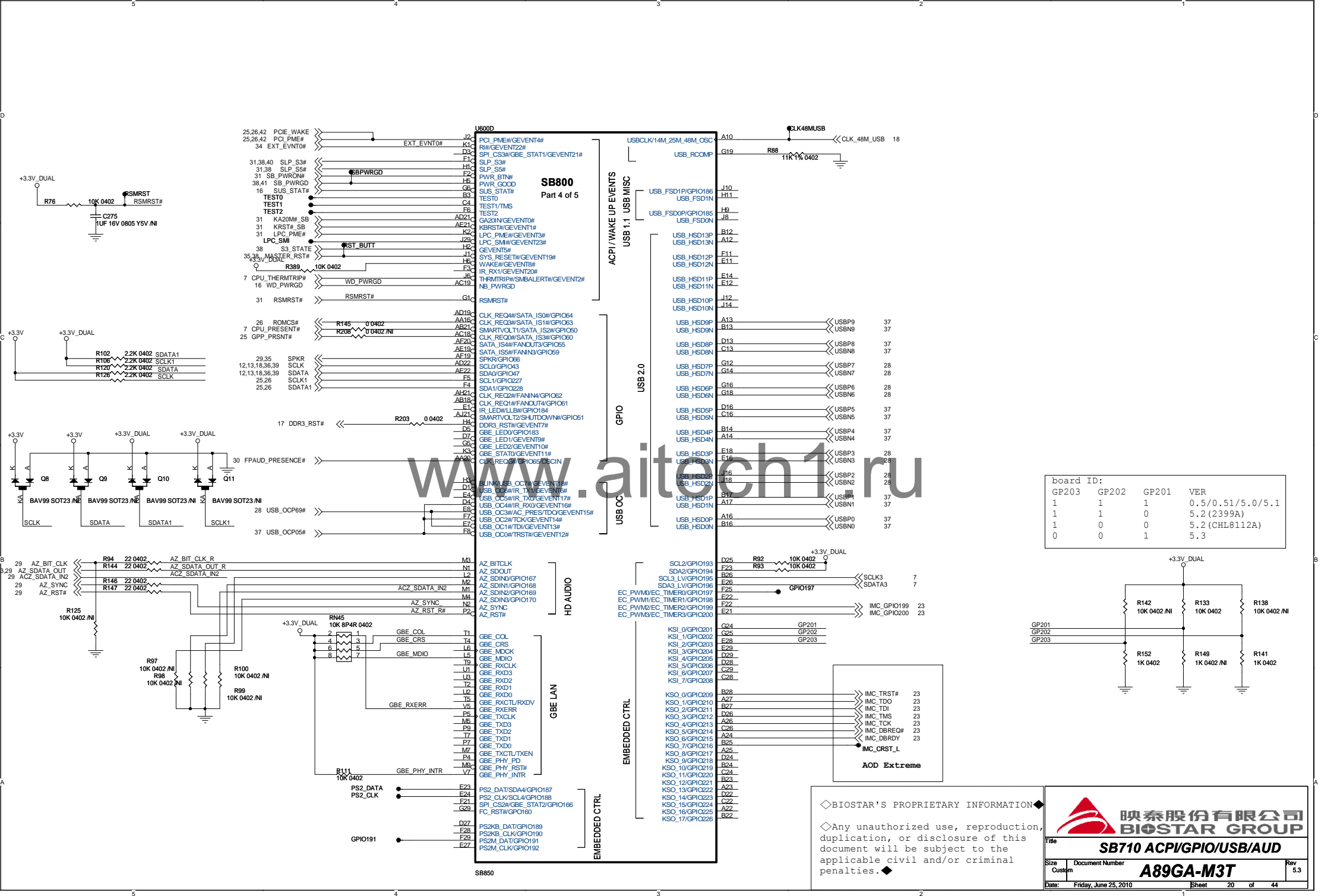
**SB710 PCIe/PCI/CPU/LPC**

**A89GA-M3T**

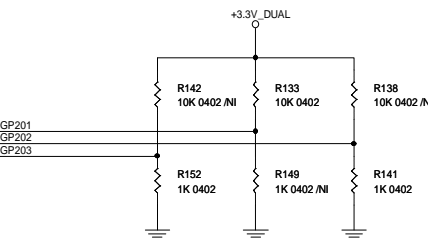
Rev 5.3

Friday, June 25, 2010

Sheet 19 of 44




board ID:			
GP203	GP202	GP201	VER
1	1	1	0.5/0.51/5.0/5.1
1	1	0	5.2 (2399A)
1	0	0	5.2 (CHL8112A)
0	0	1	5.3



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20

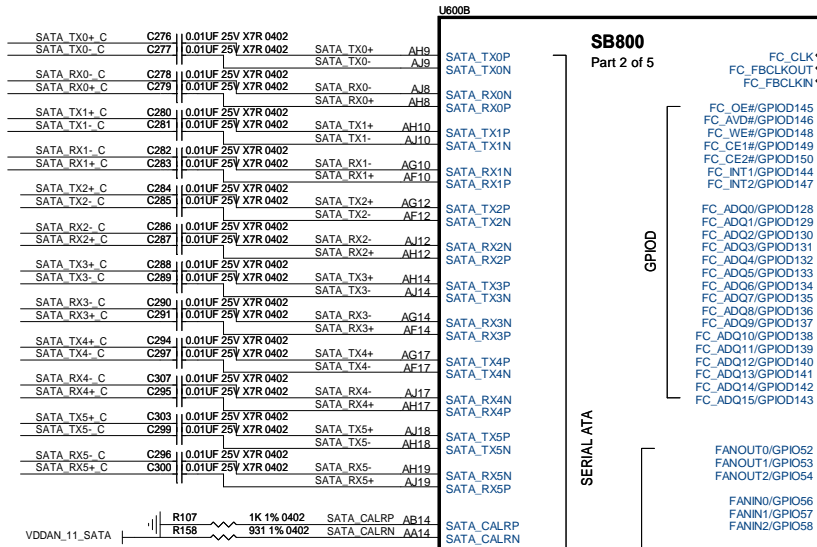
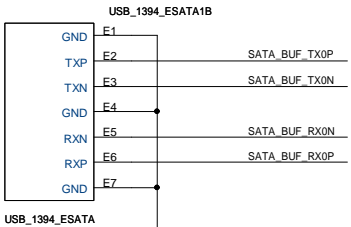
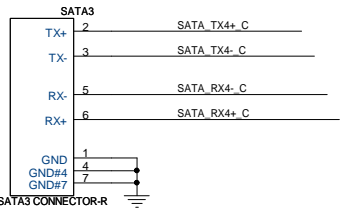
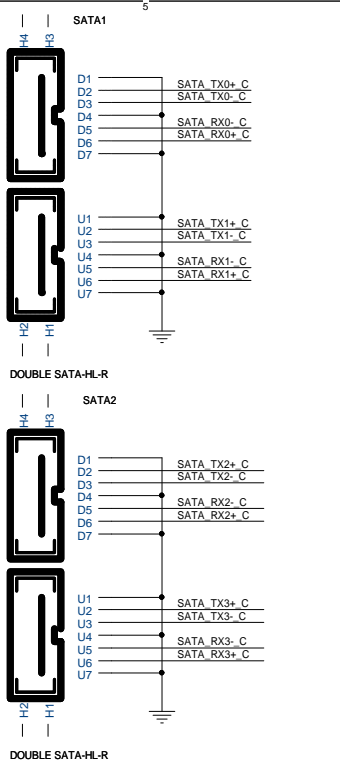
of

44

Rev

5.3





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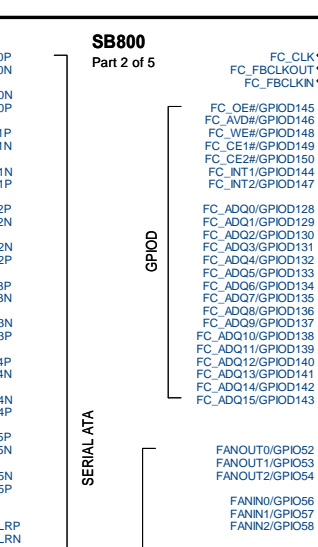
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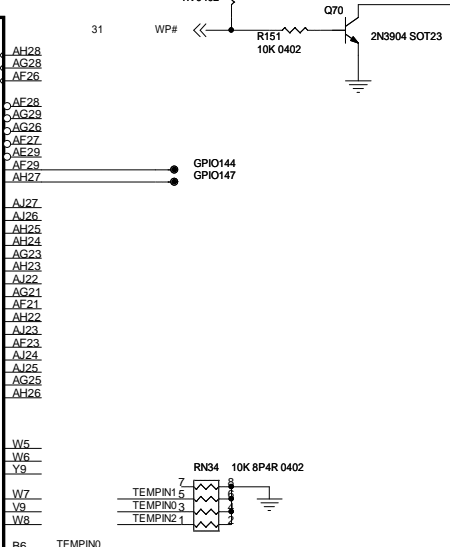
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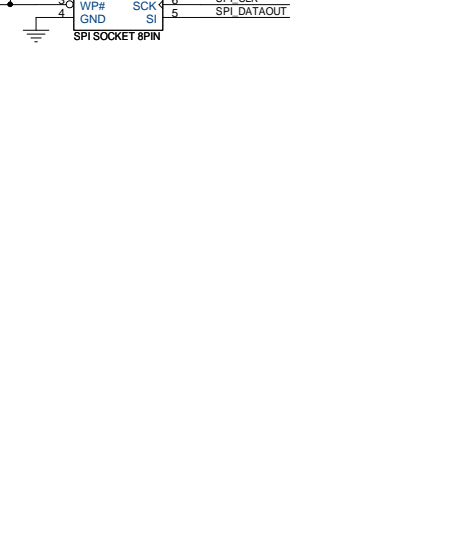
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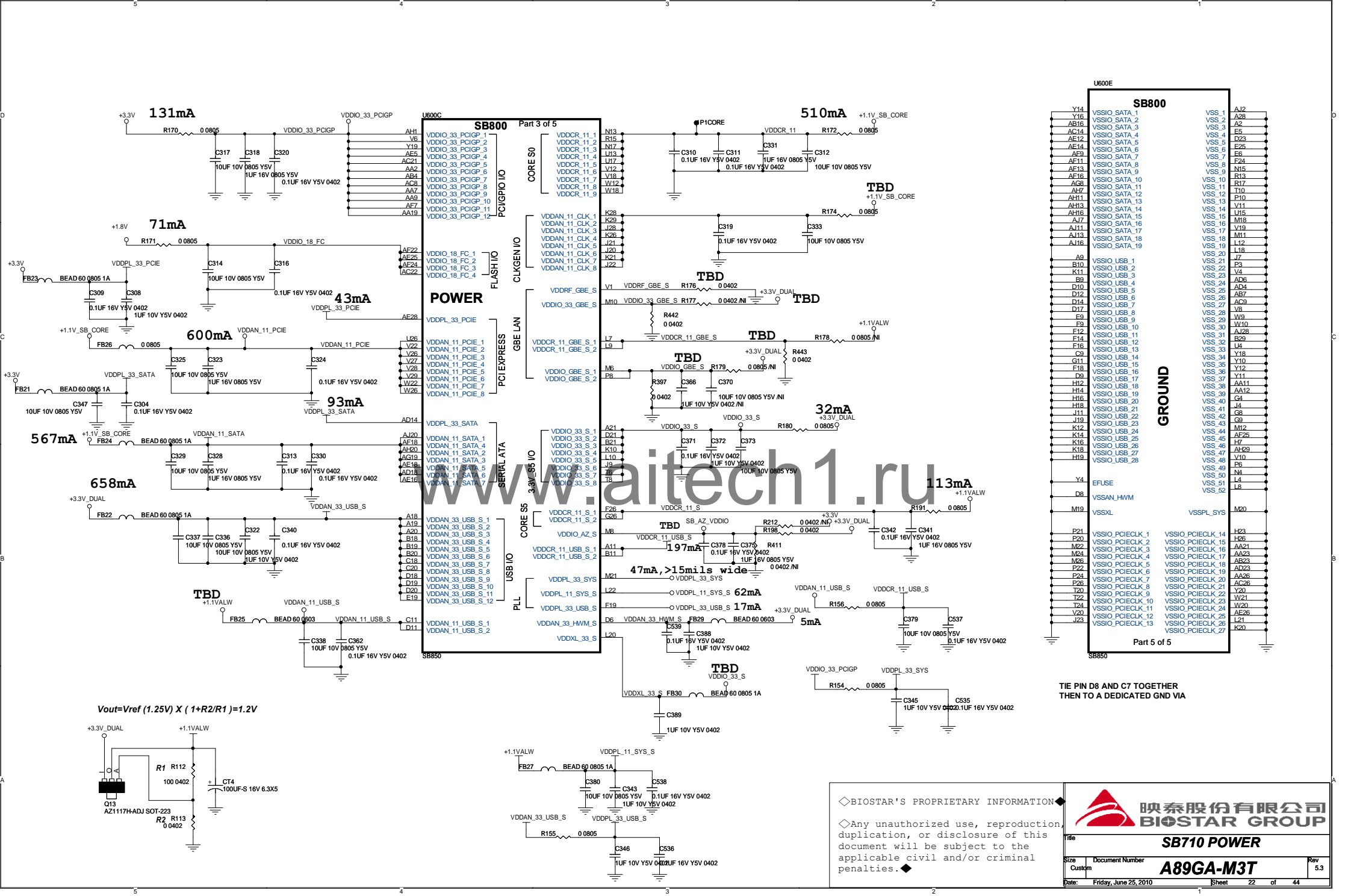
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Title **SB710 SATA/IDE/SPI**

Size Custom Document Number **A89GA-M3T** Rev 5.3

Date: Friday, June 25, 2010 Sheet 21 of 44

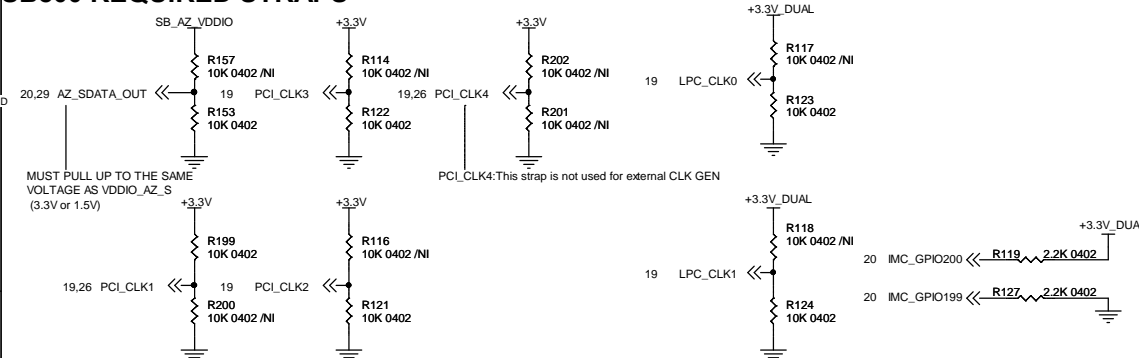




OVERLAP COMMON PADS WHERE  
POSSIBLE FOR DUAL-OP RESISTORS.

PLACE STRAP RESISTORS DIRECTLY  
ON CLK NETS (WITHOUT STUBS).

## SB800 REQUIRED STRAPS

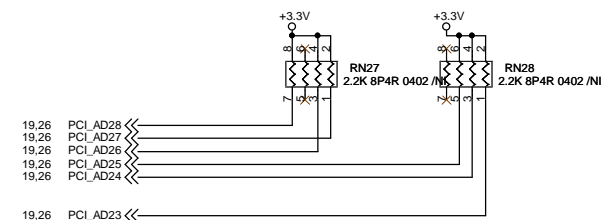


	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	NON-FUSION CPU CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM	DEFAULT
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER ON NB_PWRGD DISABLED	IGNORE DEBUG STRAPS DEFAULT	FUSION CPU CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM	

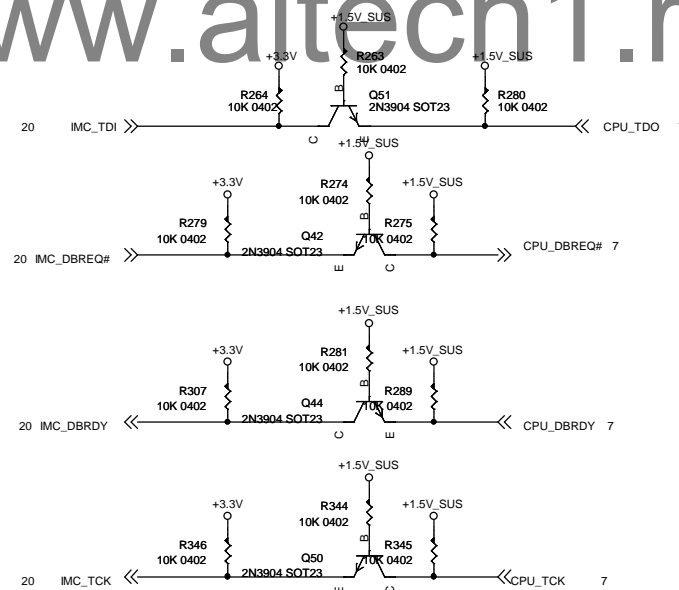
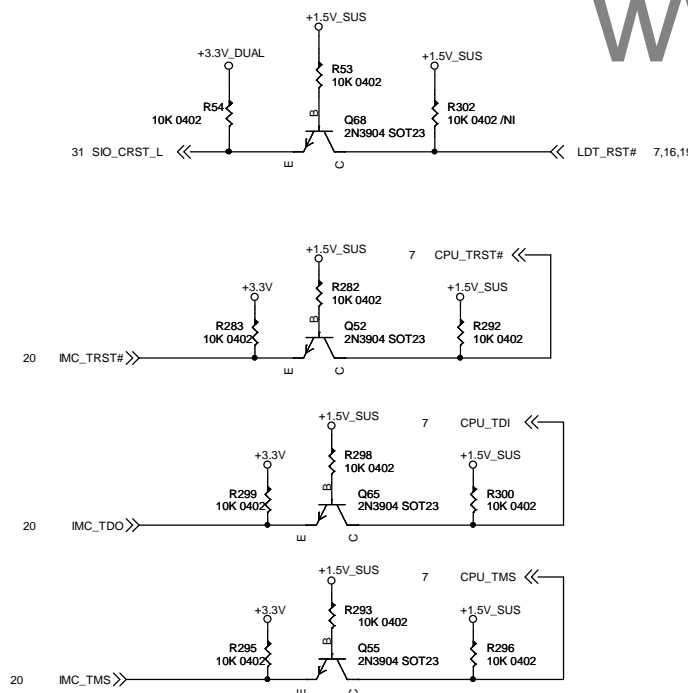
## SB800 DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI\_AD[30:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
PULL LOW	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT



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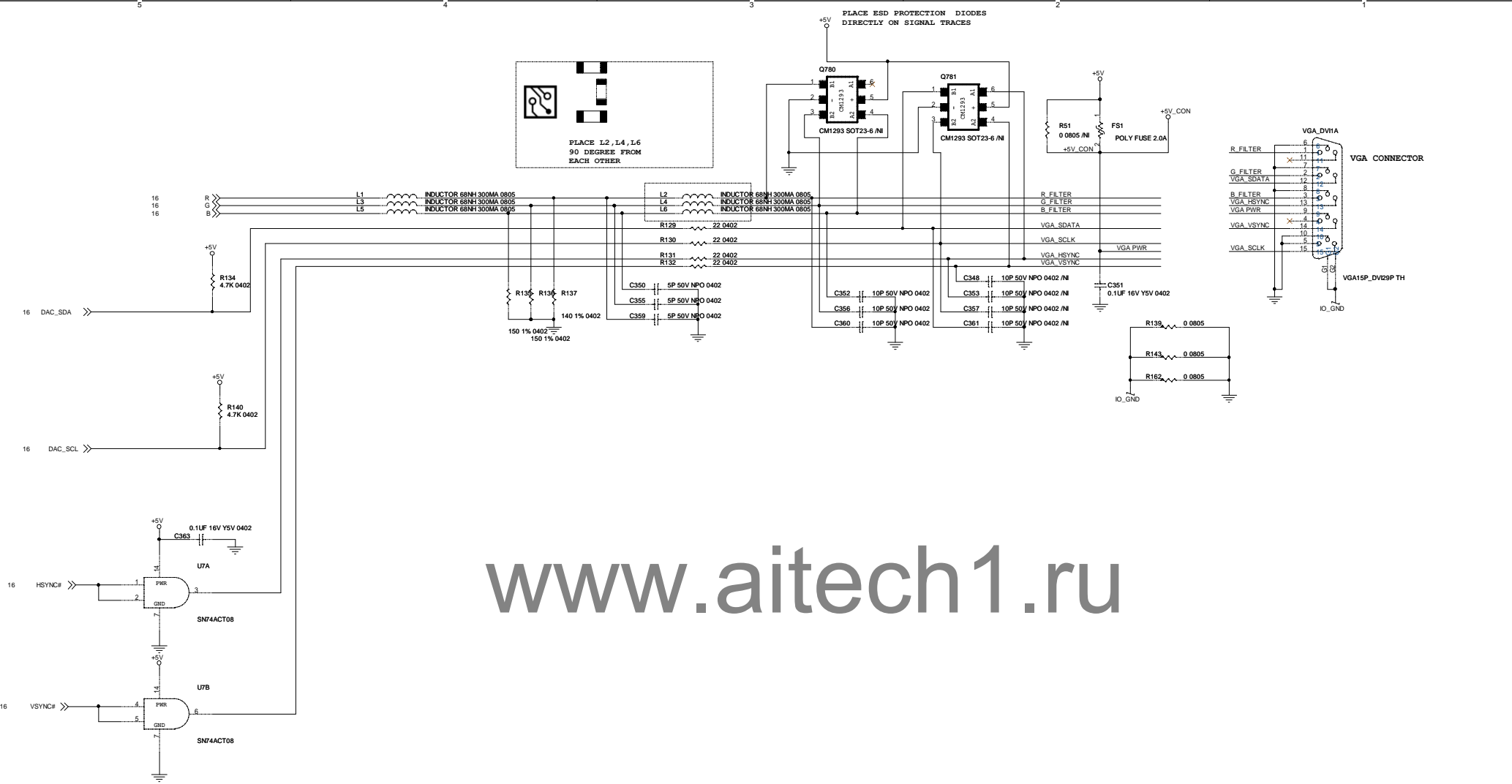


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**SB710 STRAP**


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Date: Friday, June 25, 2010 Sheet: 23 of 44



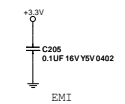
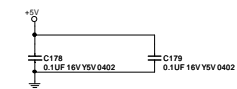
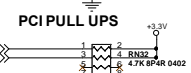
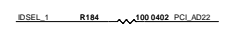
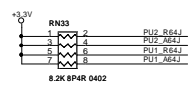
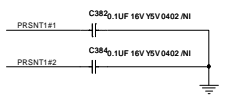
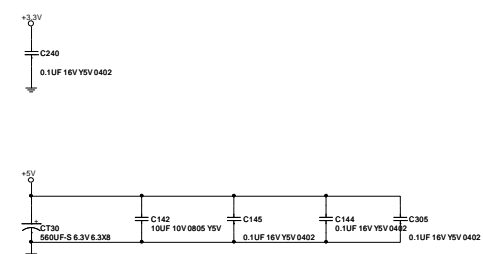
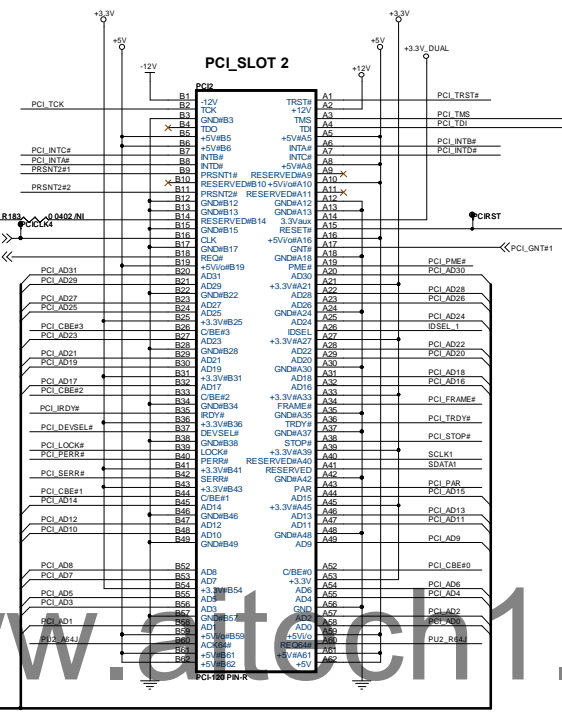
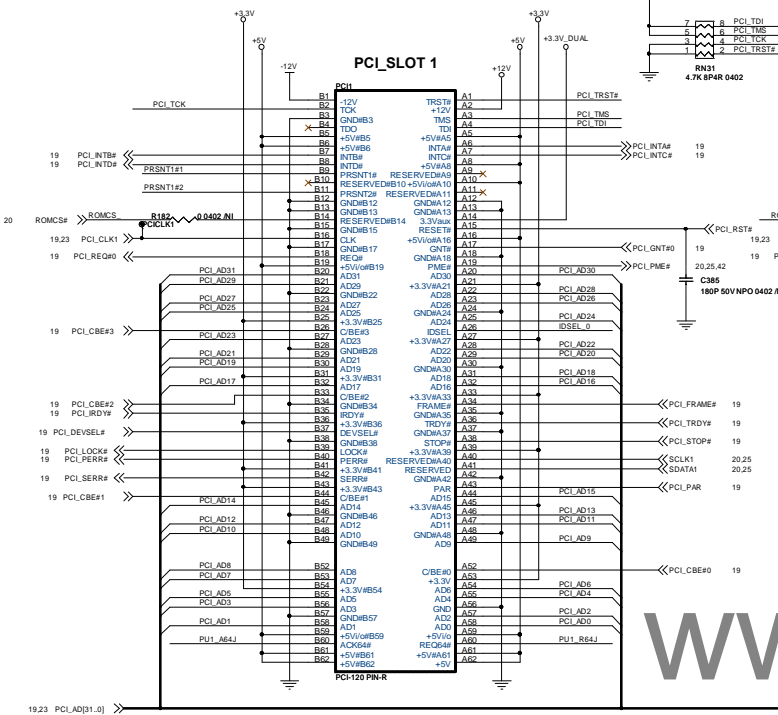
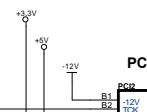
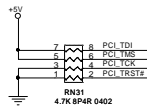
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File <b>DVI &amp; CRT</b>		
Size <b>C</b>	Document Number <b>A89GA-M3T</b>	Rev <b>5.3</b>
Date: Friday, June 25, 2010		Sheet 24 of 44



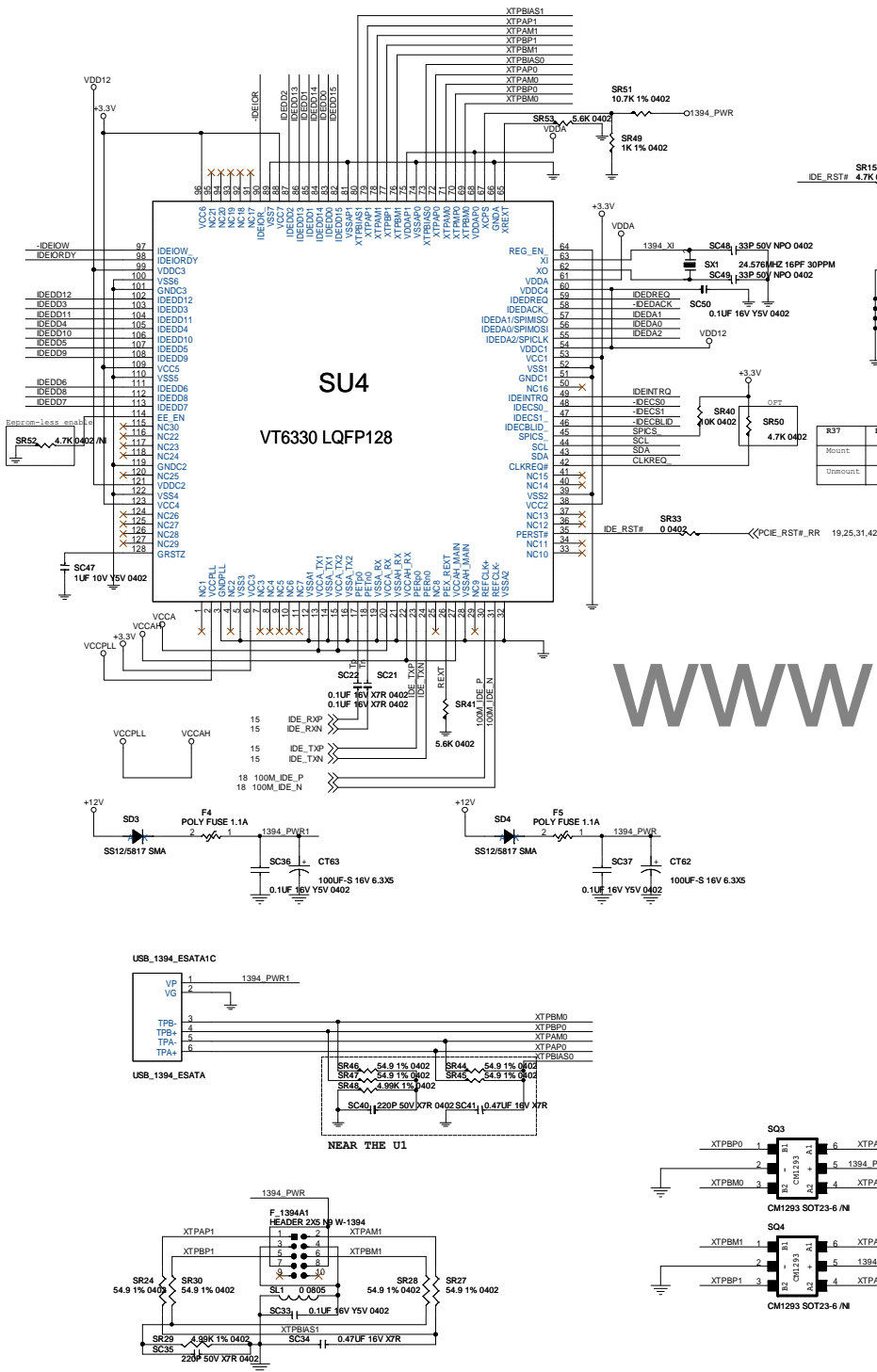


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Title				<b>PCI SLOT 1/2</b>			
Size	Document Number						Rev
Custom	<b>A89GA-M3T</b>						<b>5.3</b>
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IDE ATA 133

A89GA-M3T

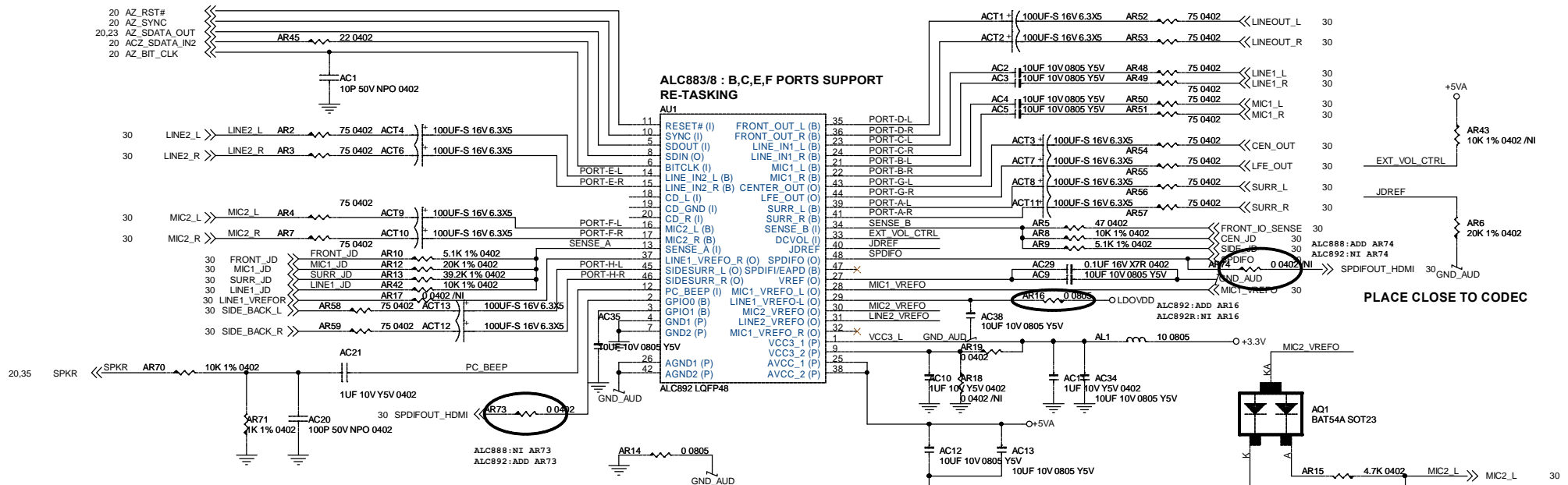
Rev 5.3

File	Document Number	Rev
Size	Custom	5.3
Date	Friday, June 25, 2010	Sheet 27 of 44

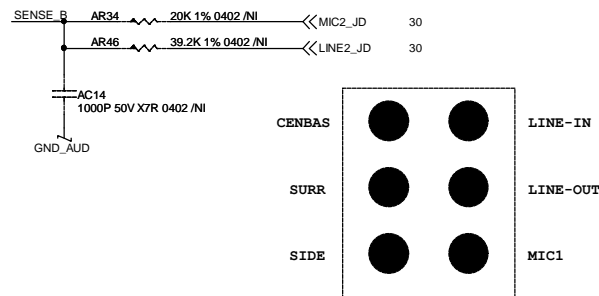
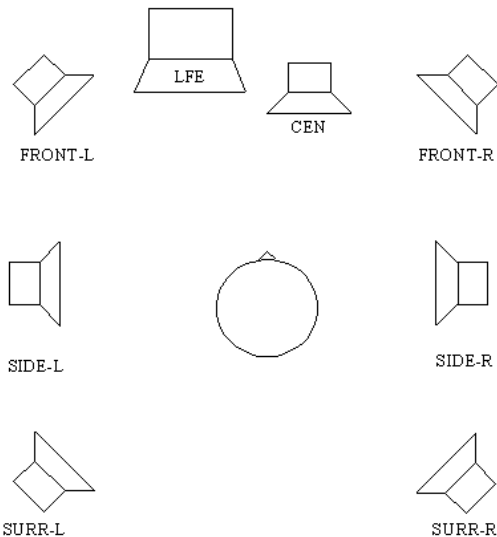








## 7.1 Speaker Configuration



Configuration

	PORT-A	PORT-B	PORT-C	PORT-D	PORT-E	PORT-F	PORT-G	PORT-H
Function	SURR	MIC1	LINE1	LINEOUT	LINE2	MIC2	CEN/LFE	SIDE
Location	Rear	Rear	Rear	Rear	Front	Front	Rear	Rear

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Title **CODEC ALC 892**

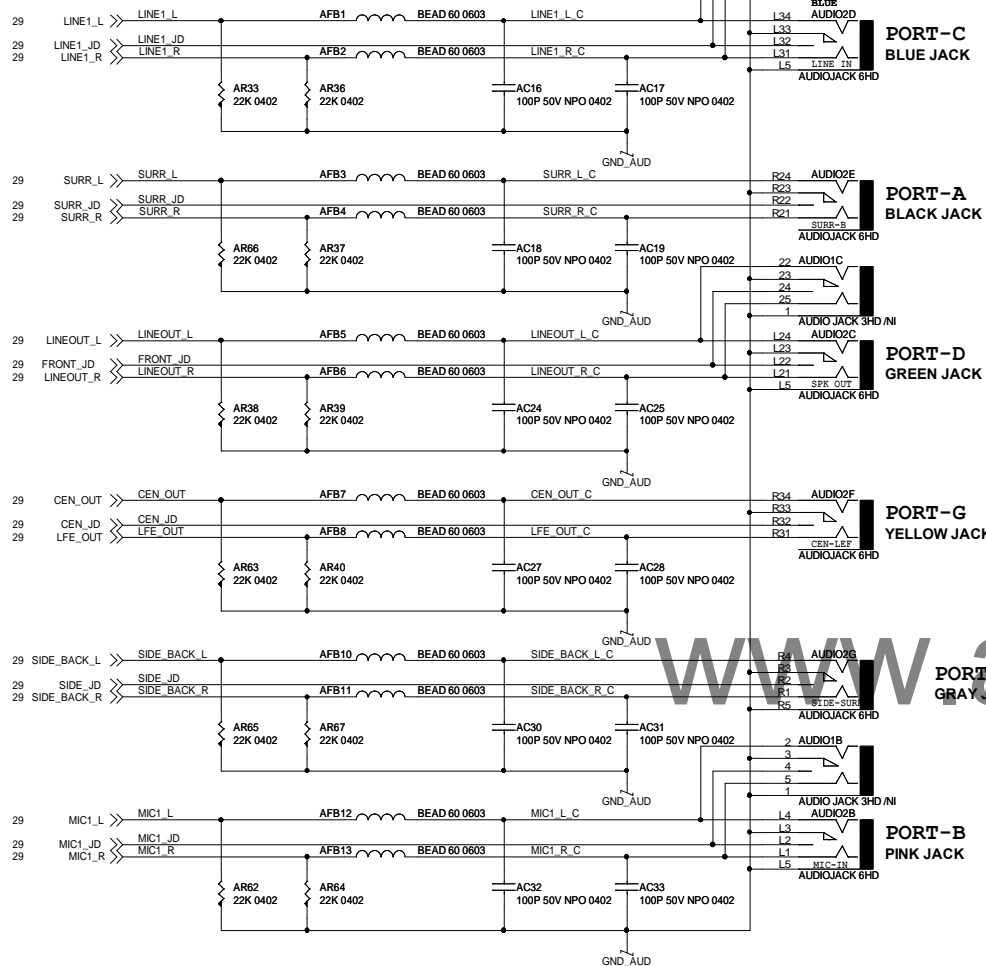
Size Document Number **A89GA-M3T** Rev 5.3

Date: Friday, June 25, 2010 Sheet 29 of 44

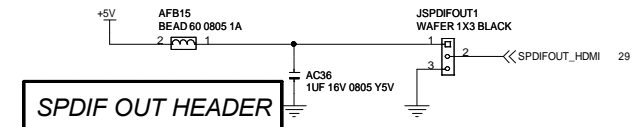
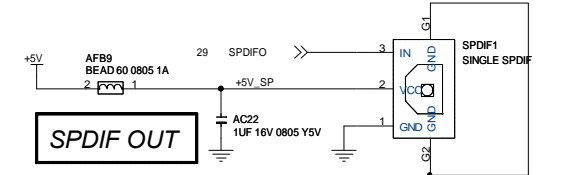
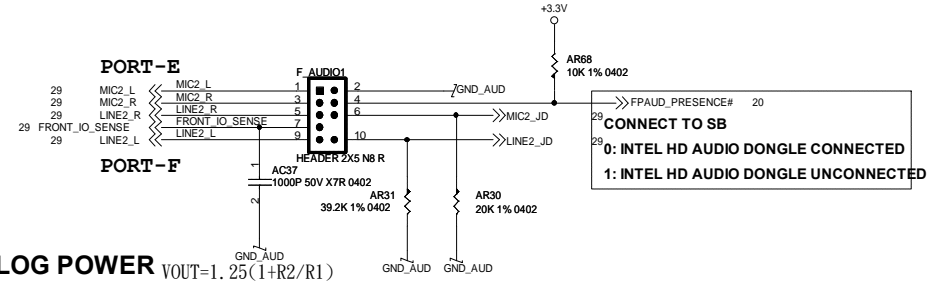
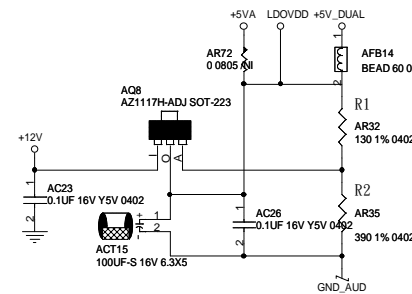
# Rear Panel Onboard Analog I/O P07 : 3-Port & 6-Port Co-lay

ALC883/888:B,C,E,F ports support I/P & O/P function.

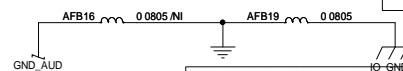
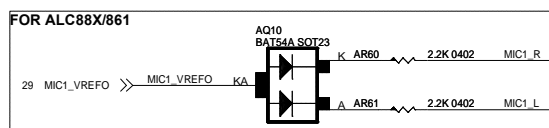
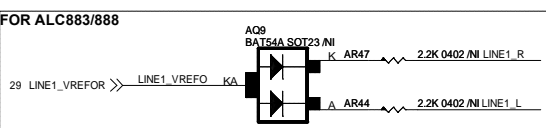
But A,D,G,H ports not support MIC function.



AUDIO ANALOG POWER  $V_{OUT}=1.25(1+R2/R1)$



	ALC883/8	ALC861VD
HDA Interface	Yes	Yes
DAC	5 DAC 7.1Ch + 2 Ch	4 DAC 7.1Ch
DAC SNR	95dB	90dB
GPIO for Vref	None	None
SPDIF-I	Yes	No
SPDIF-O	Yes	Yes
Re-Tasking	4-PORTS	Port D,E,F

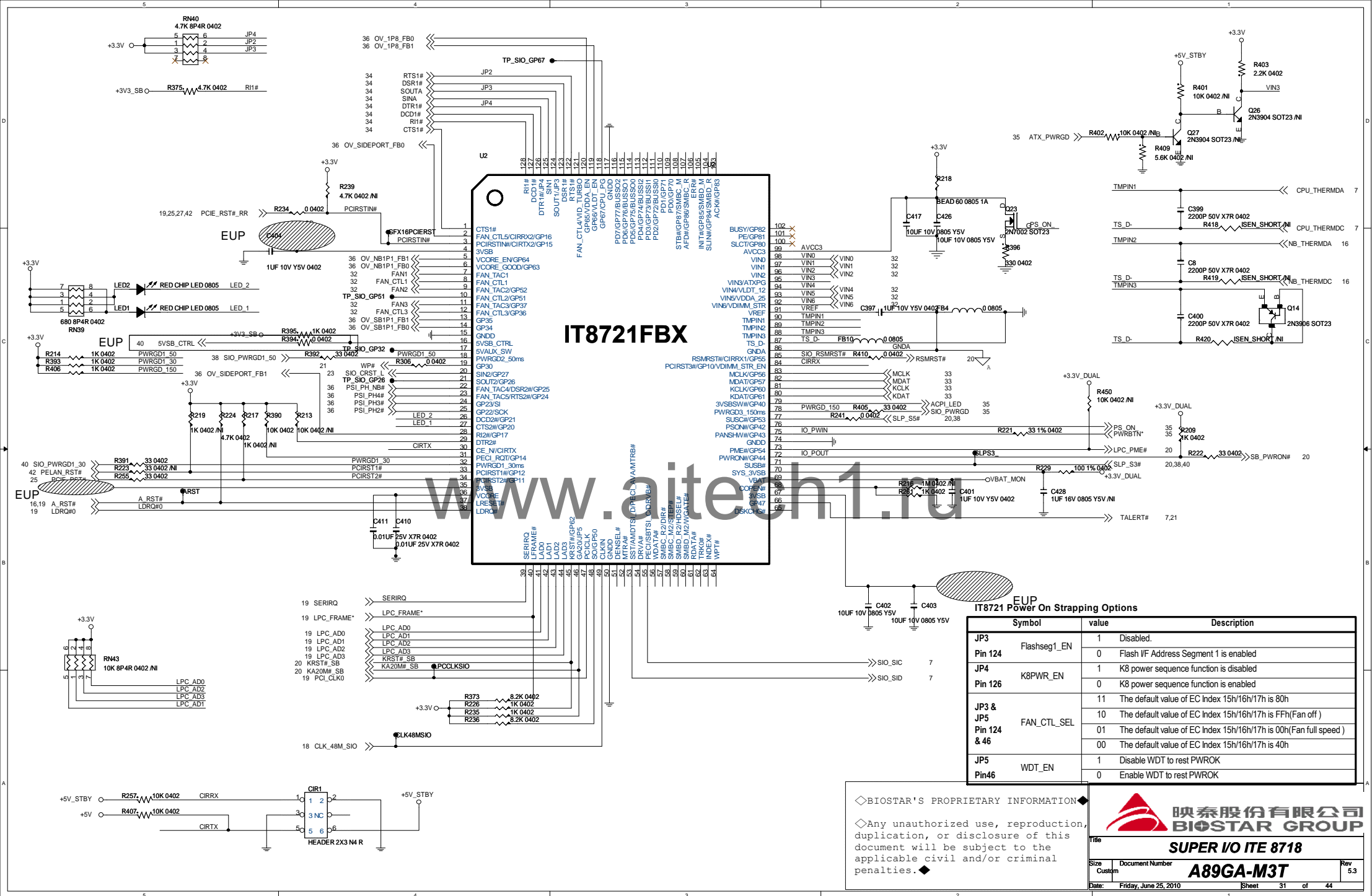


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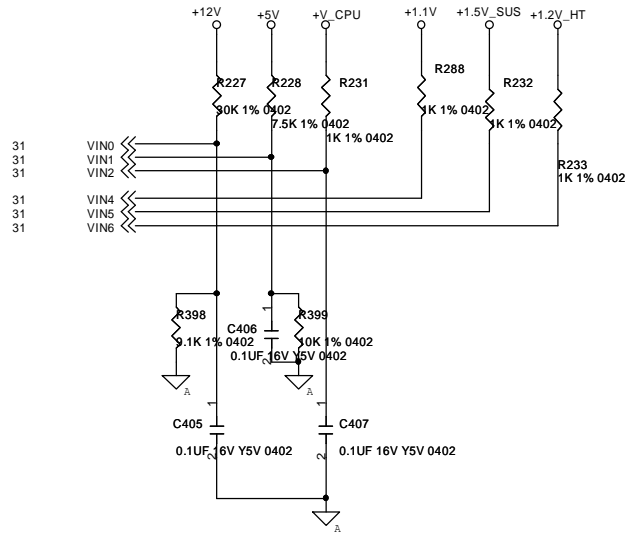
**AUDIO CONNECTOR**  
**A89GA-M3T**

Title: \_\_\_\_\_  
 Size: Custom Document Number: \_\_\_\_\_  
 Date: Friday, June 25, 2010 Sheet 30 of 44 Rev 5.3

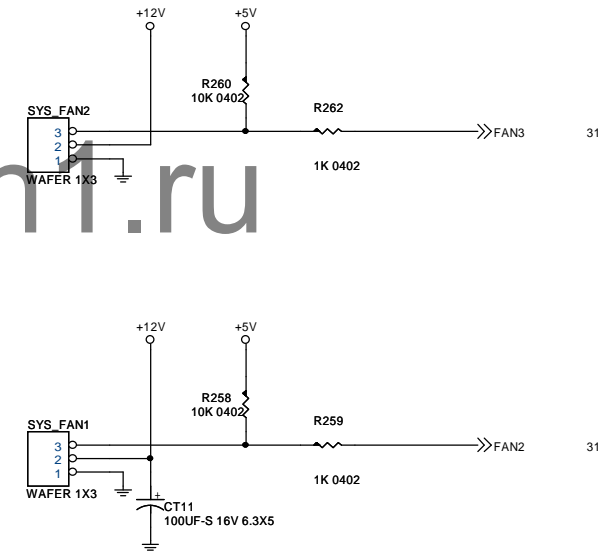
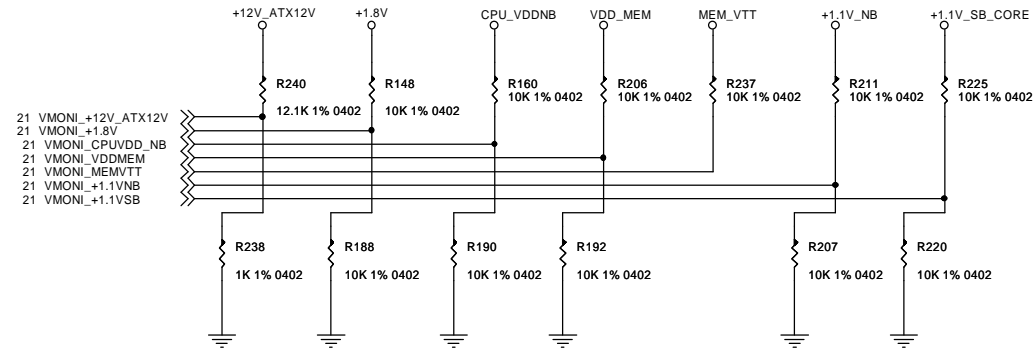


## SB800 power monitoring inputs

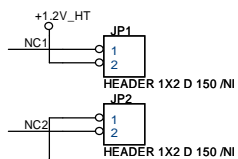
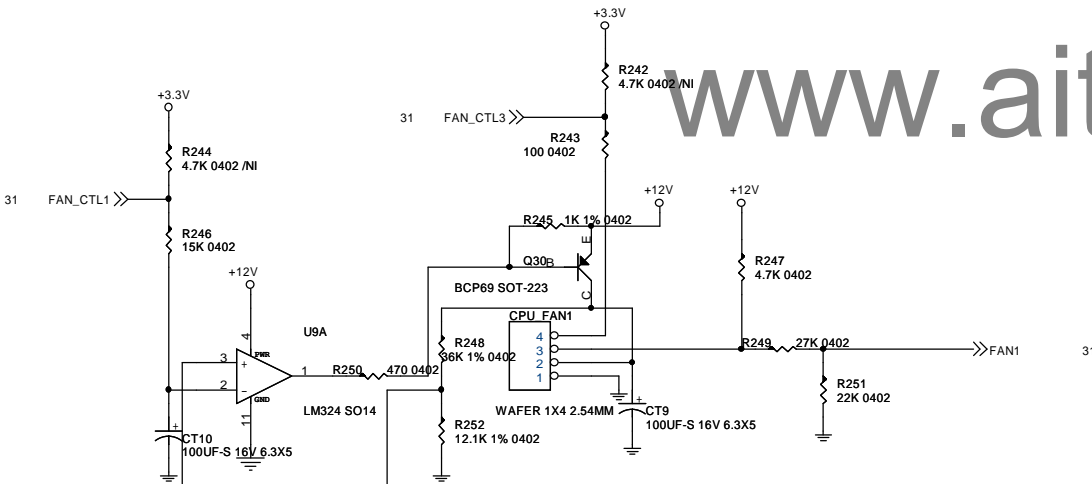
1. USE EXTERNAL RESISTOR DIVIDER IF INPUT VOLTAGE IS LARGER THAN 1.0V
2. MAKE SURE THE CENTER VOLTAGE IS 0.9V IF USE EXTERNAL DIVIDER, IF THE RAIL ALLOWS OVERVOLTAGE, SET THE CENTER VOLTAGE TO 0.5V



Note: The division voltage of VIN0 and VIN1 must be around 2.8V




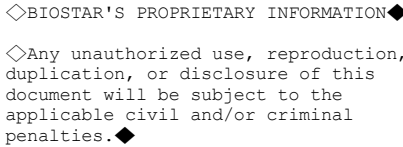
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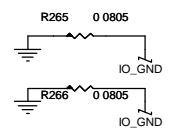
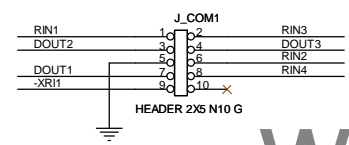
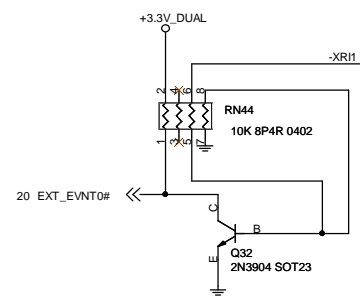
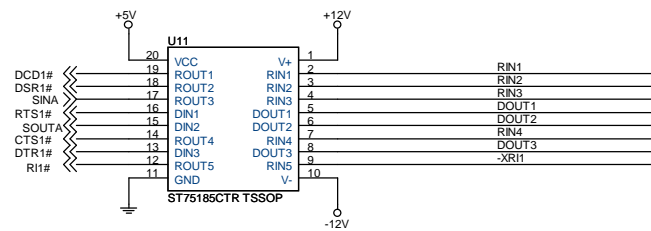
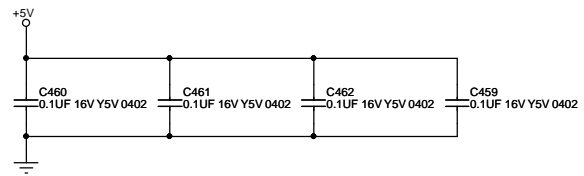
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<b>Title</b> HW MON/FAN CONTROL	
<b>Size</b> Custom	<b>Document Number</b> A89GA-M3T
<b>Date:</b> Friday, June 25, 2010	
<b>Sheet</b> 32 of 44	
<b>Rev</b> 5.3	




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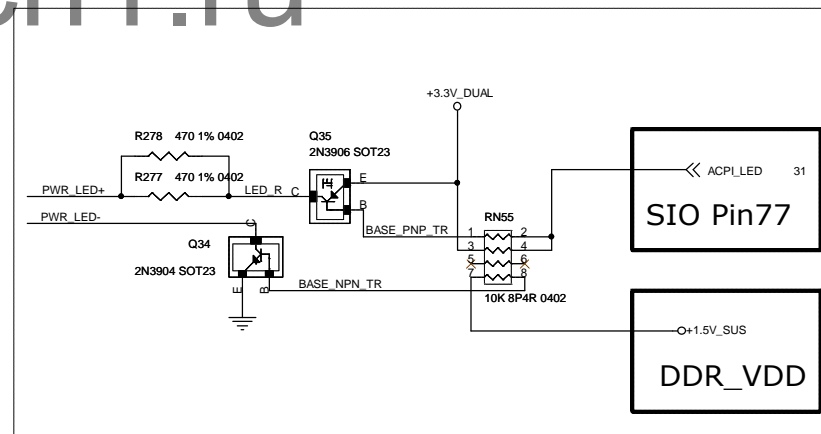
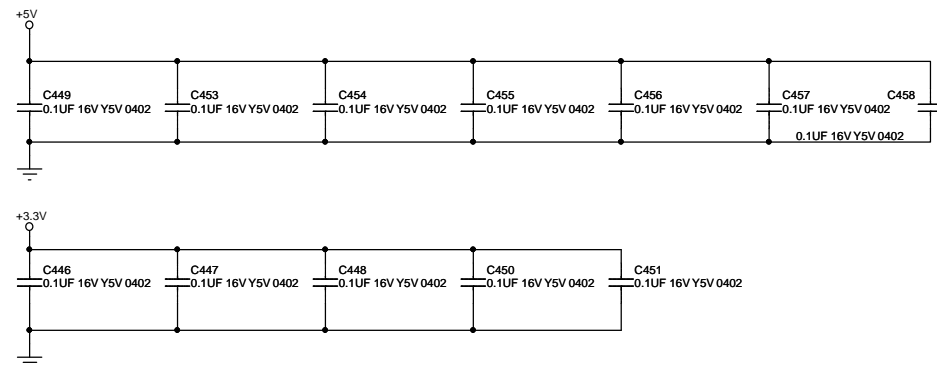
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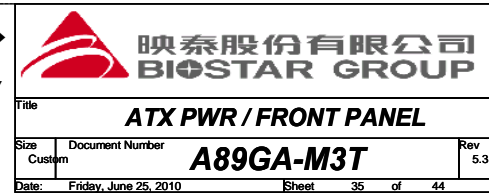


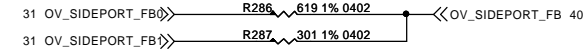
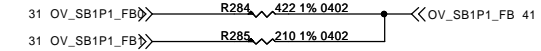
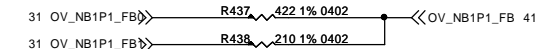
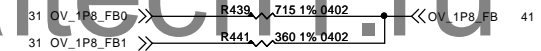
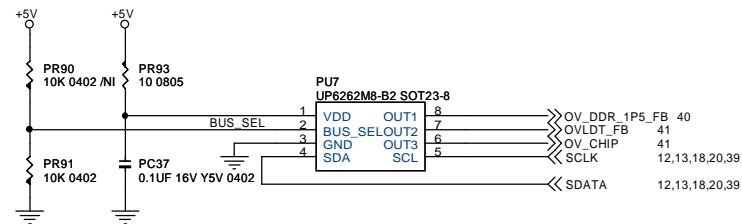
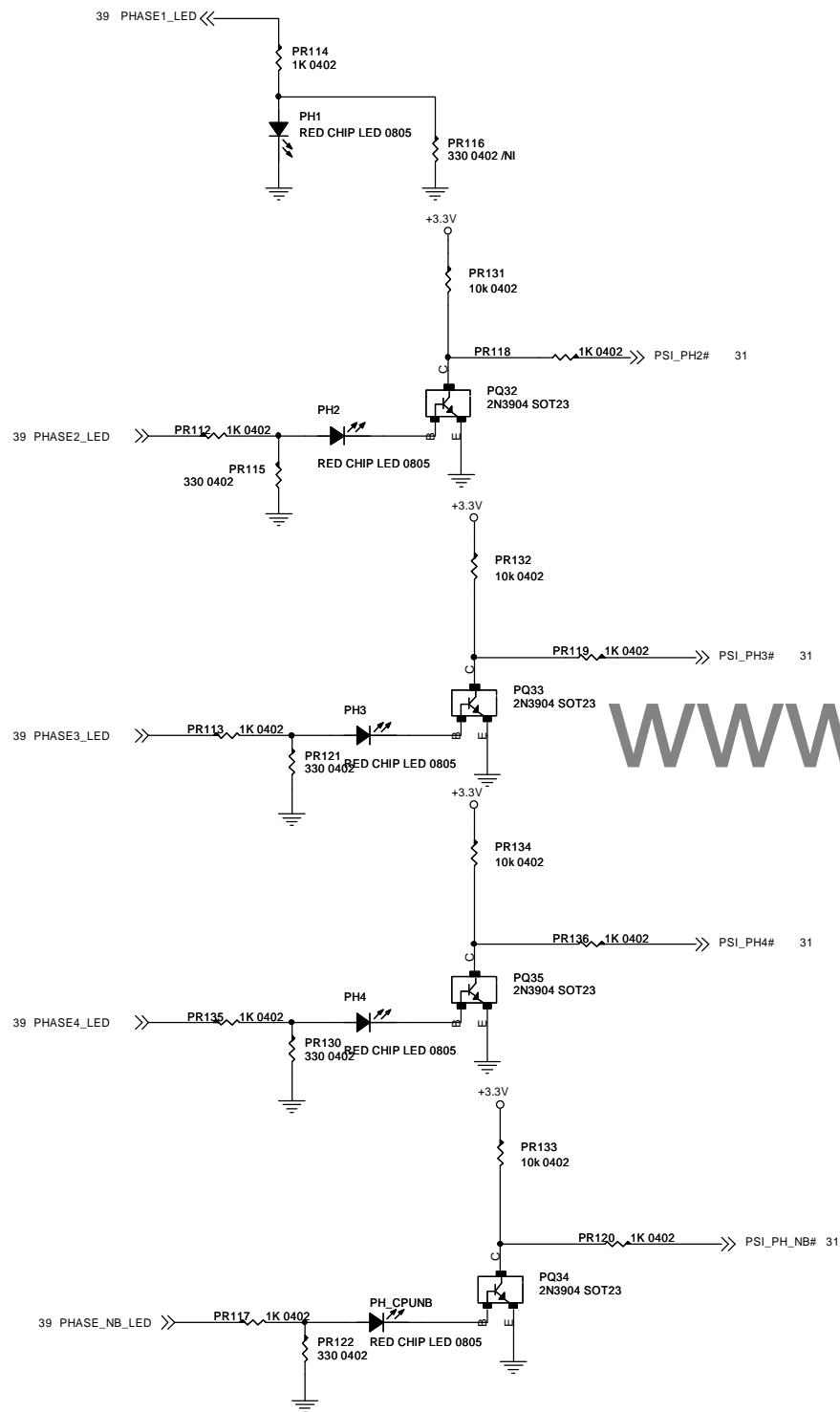
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Title		COMPORT/PRINT HEADER	
Size	Document Number	Rev	
Custom	A89GA-M3T	5.3	
Date:	Friday, June 25, 2010	Sheet	34 of 44



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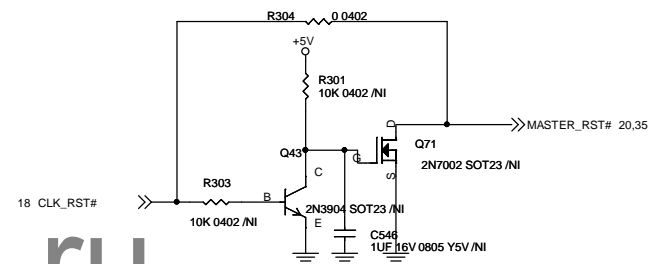
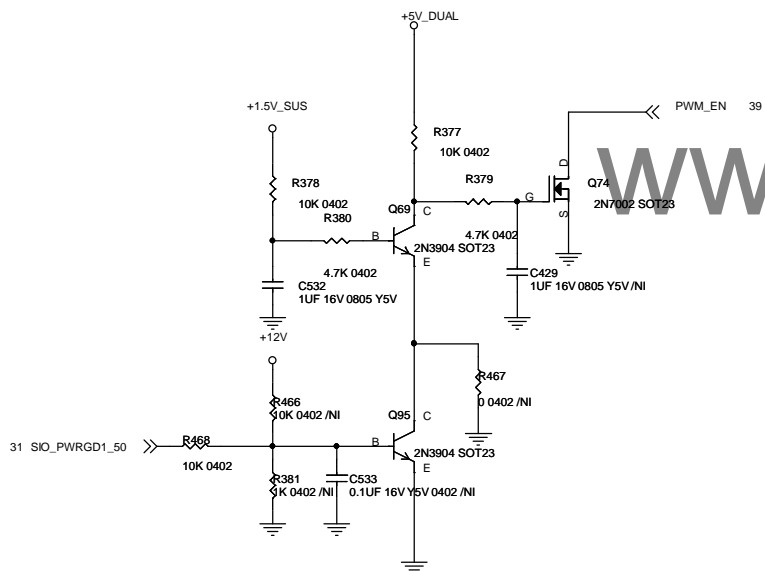
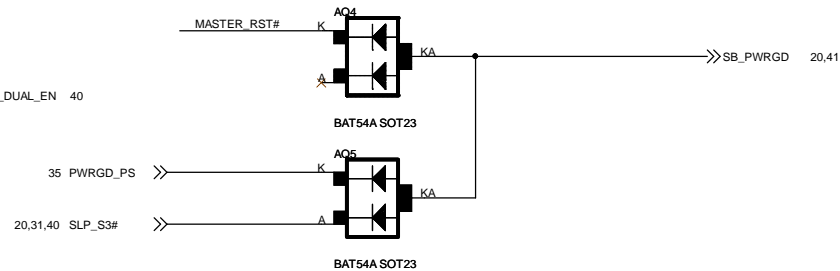
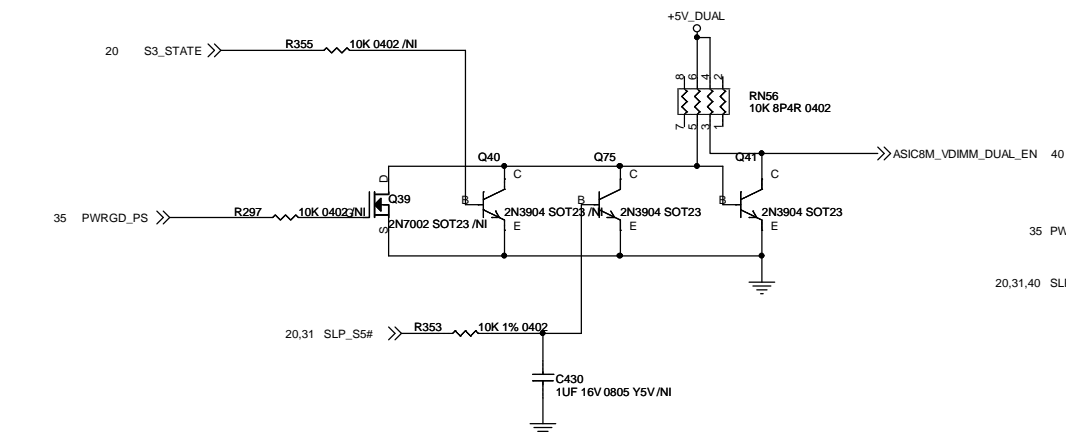
Date: Friday, June 25, 2010

Rev 5.3

Sheet 36 of 44






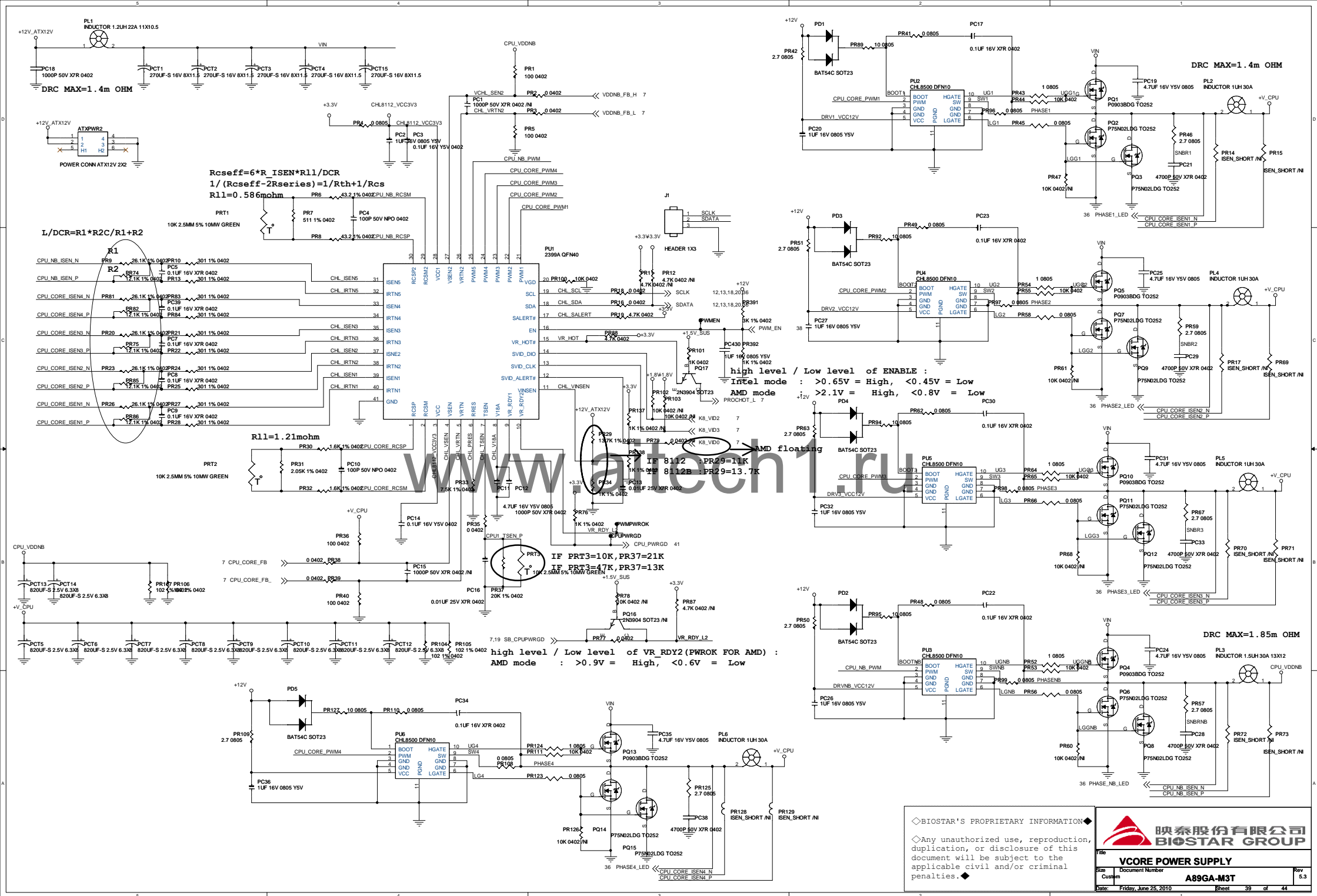


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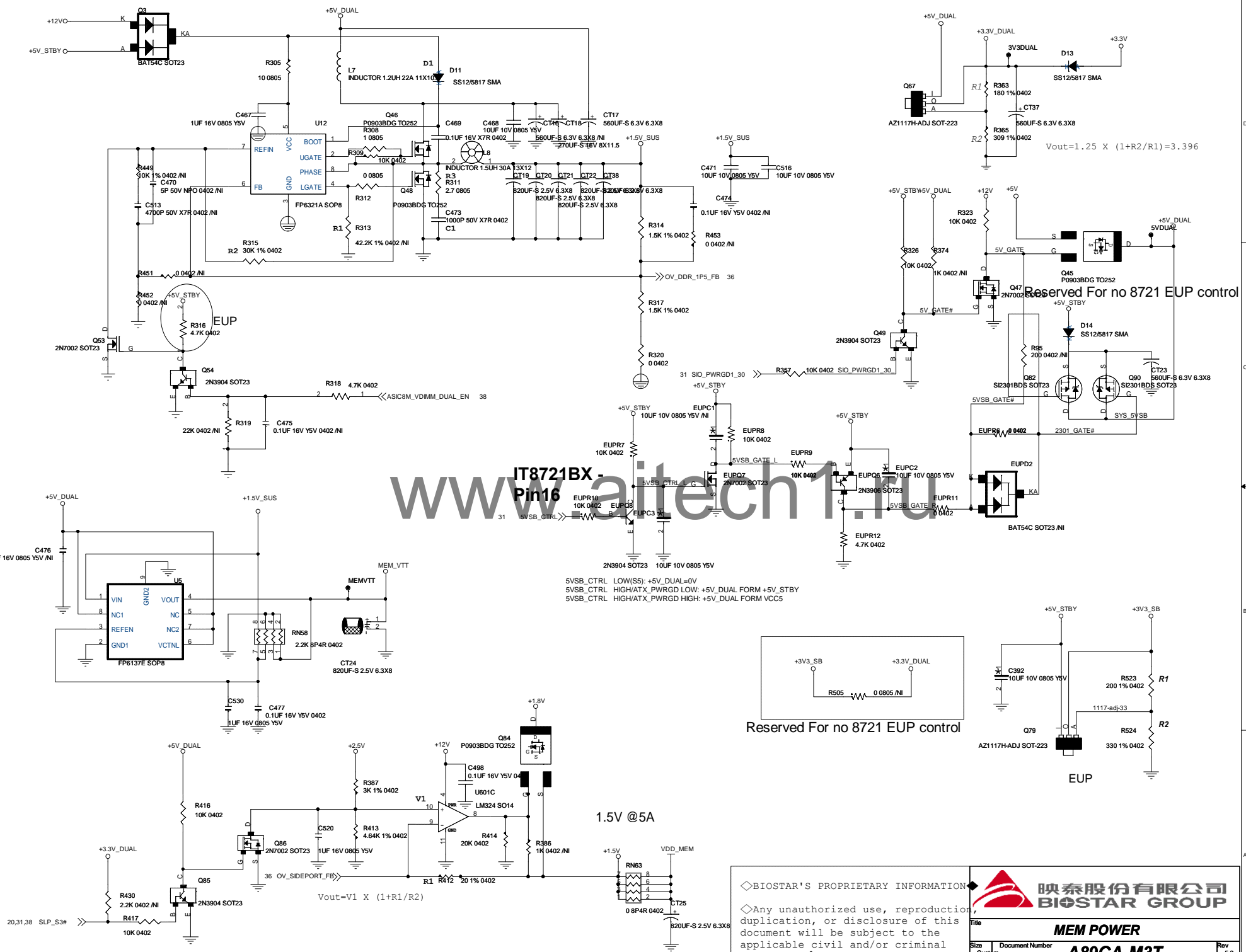
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Date: Friday, June 25, 2010	Rev 5.3
Sheet 38 of 44	



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INDUCTOR 4.7uH 1.3A DFP

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LR6 R2 0.0805

EVDD12

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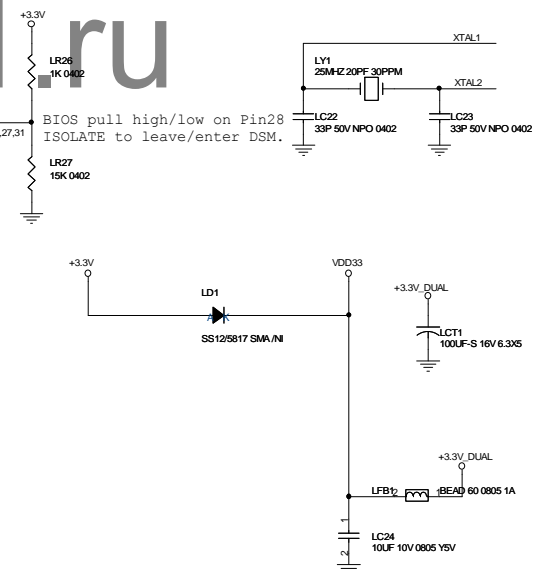
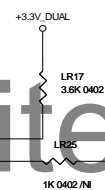
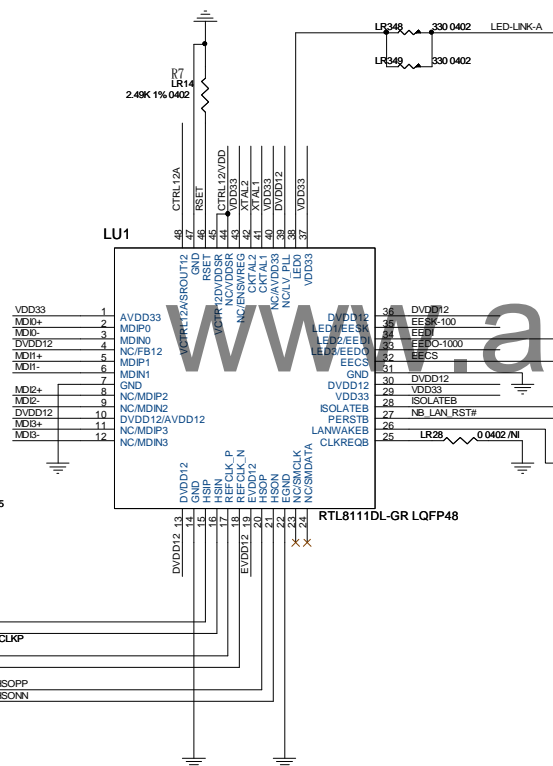
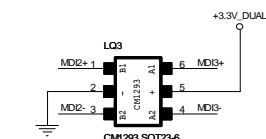
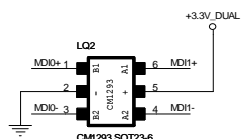
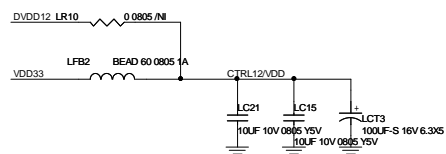
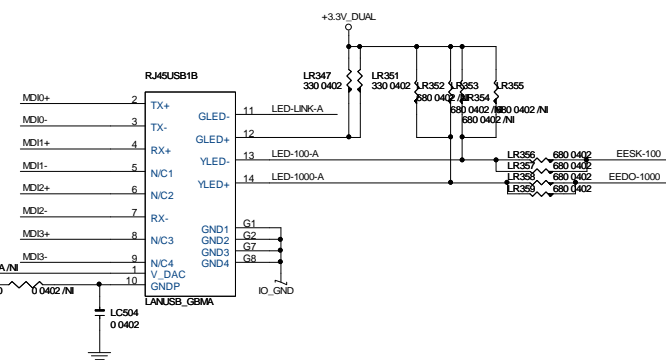
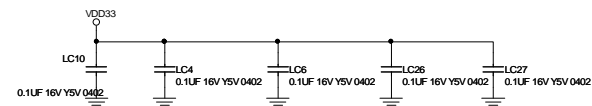
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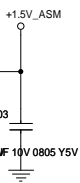
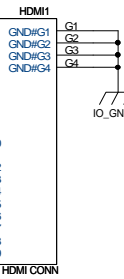
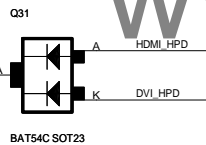
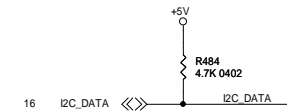
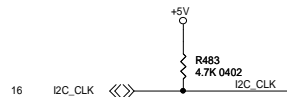
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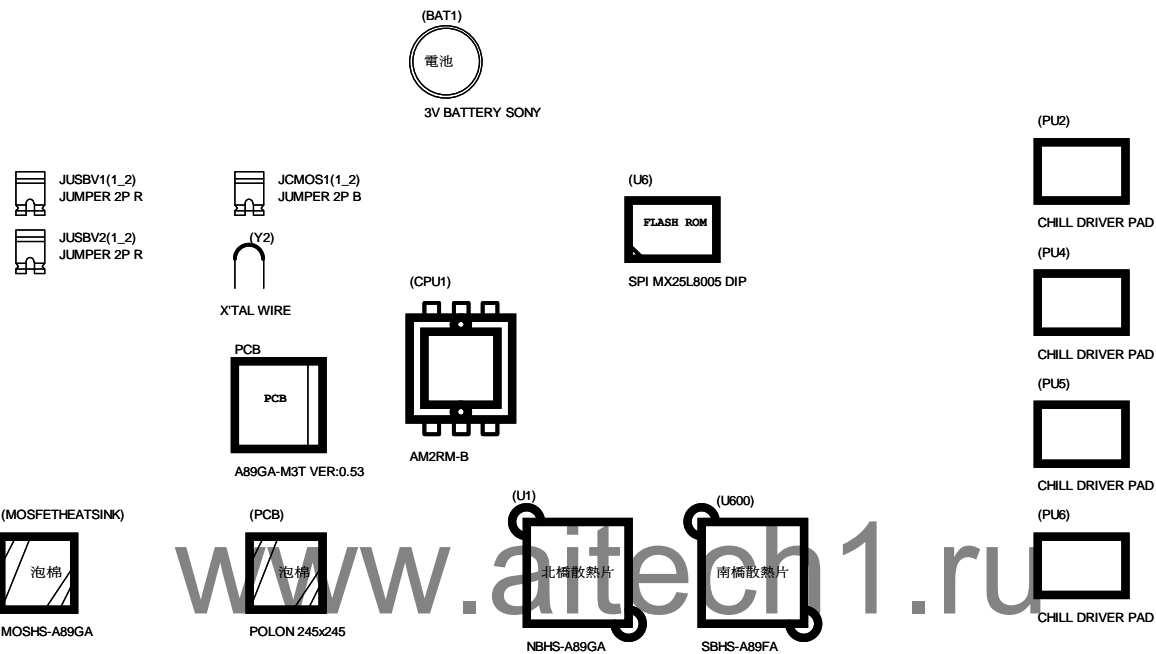


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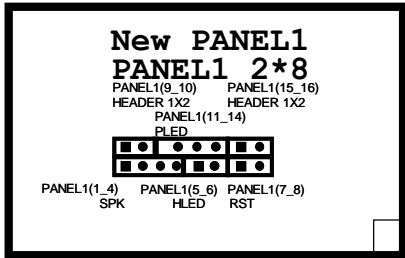


Title			
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Size	Document Number		Rev
Custom	A89GA-M3T		5.3
Date:	Friday, June 25, 2010	Sheet	42 of 44






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Size B	Document Number A89GA-M3T		Rev 5.3
Date: Friday, June 25, 2010		Sheet 44	of 44